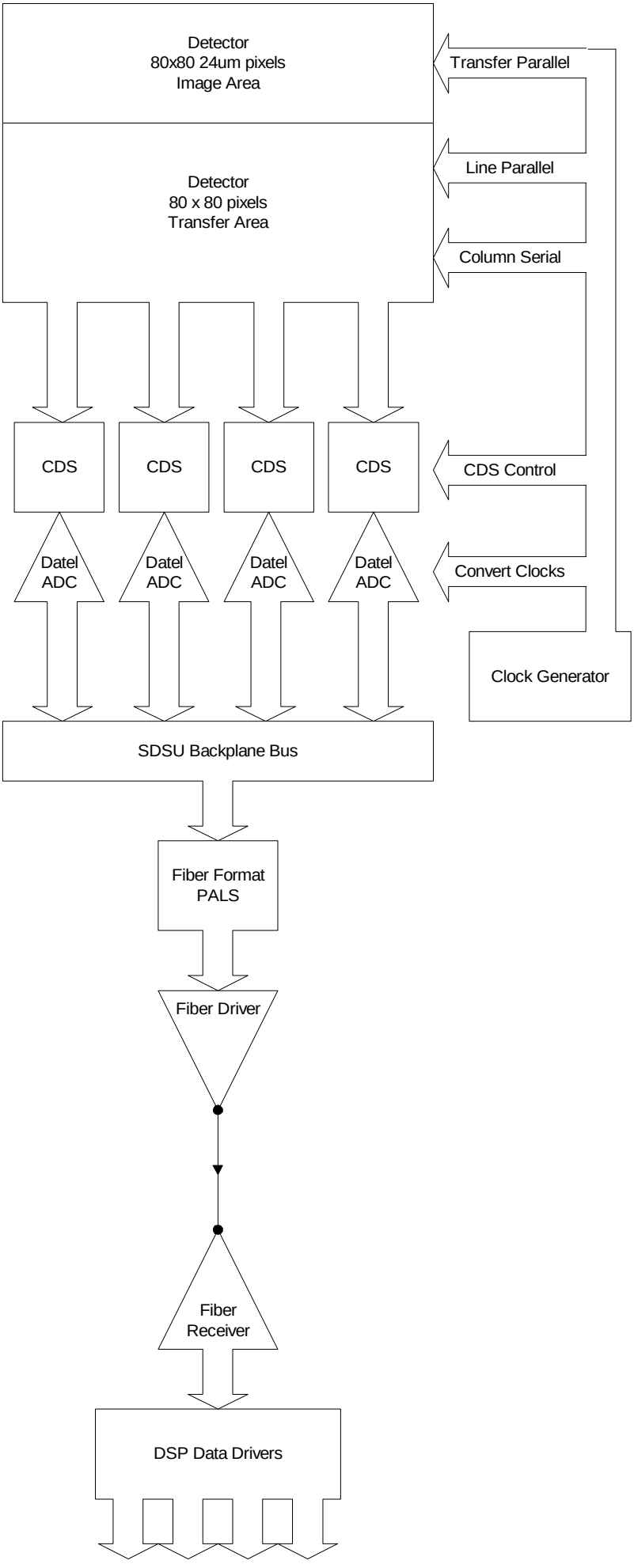

DETECTOR

CCD39 - 01
90% QE @ 500nm
55% QE @ 800nm

3e- RMS @ 40K Pixel/Sec
6e- RMS @ 1M Pixel/Sec

Require 72 Subapertures of
6 x 6 pixels = 2592 pixels.

Total pixels = 6400.
Maximum Clocking Rate > 6Mhz.
Maximum Pixel Rate > 3MPix/Sec x 4
Equivelent to 12MPix/Sec.

SDSU CONTROLLER

Corrolated Double Sampler
400ns sample possible allowing
1 us/pixel x 4 = 4Mpix/Sec.

Analog to Digital Converters
DATEL 1 Msample Converters
4 converters = 4 MPix/Sec.

Clock Generator and Timing
20ns Resolution.
60ns nominal rise time for clock line.
Need 4 overlap clocks per pixel
Therefore 2.77 Million Cycles/Sec x 4
Equivelent to 11 MPix/Sec.

Data Transport

Zero intermediate data storage limits transfer to data link speed i.e for a 4 channel system this is 2.7 MPix / 4 = 675KPix/Sec.

DATA LINK

50 MBit / Sec.
Data Format 16 Bits + start = 17 Bits
+ Framing Recovery Time
Therefore
Max Practicle Pixel rate = 2.7 MPix / Sec.

DATA FORMATTER

Limited by Receiver Bit Rate.
i.e 2.7 MPix/Sec.