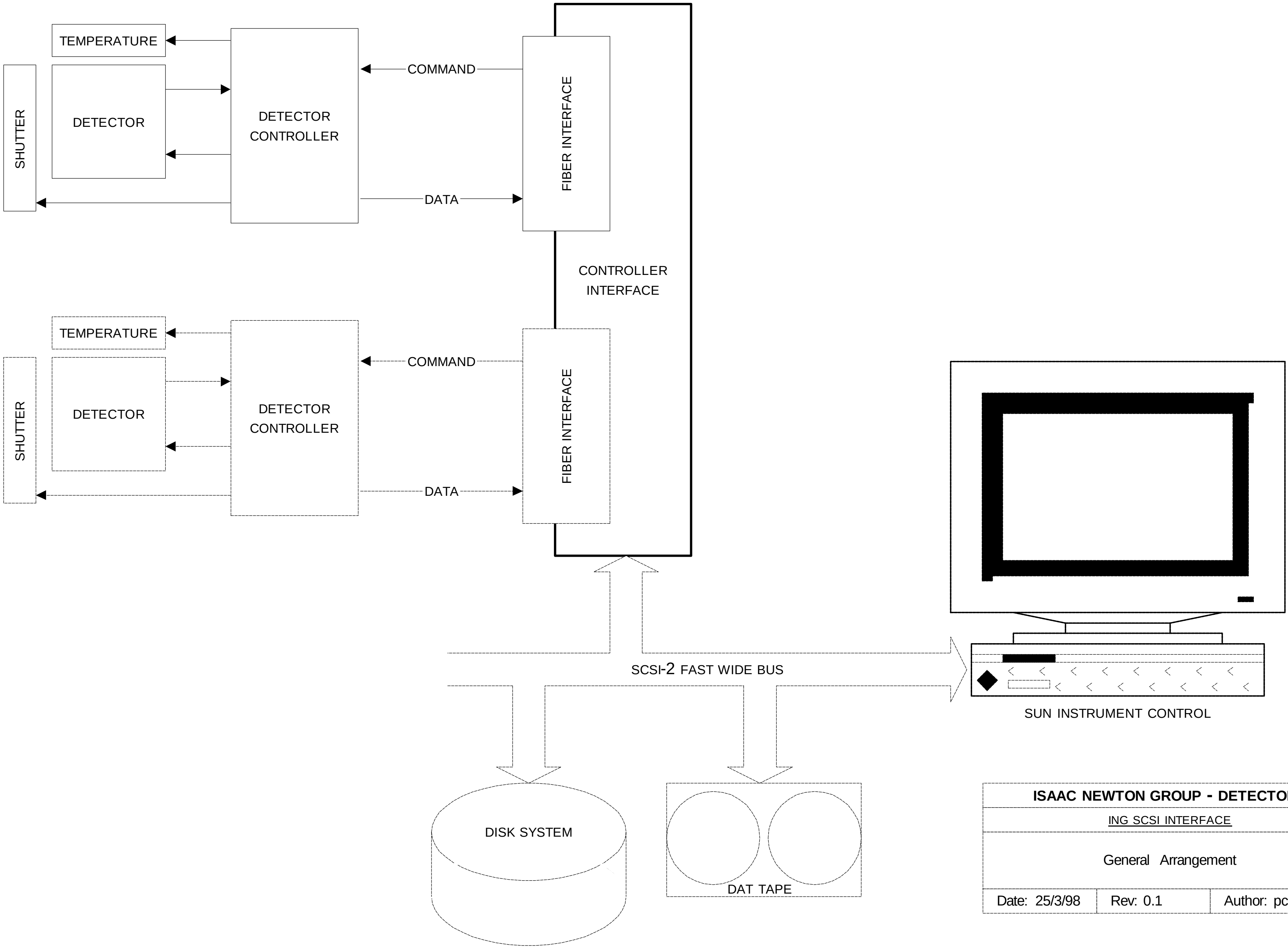
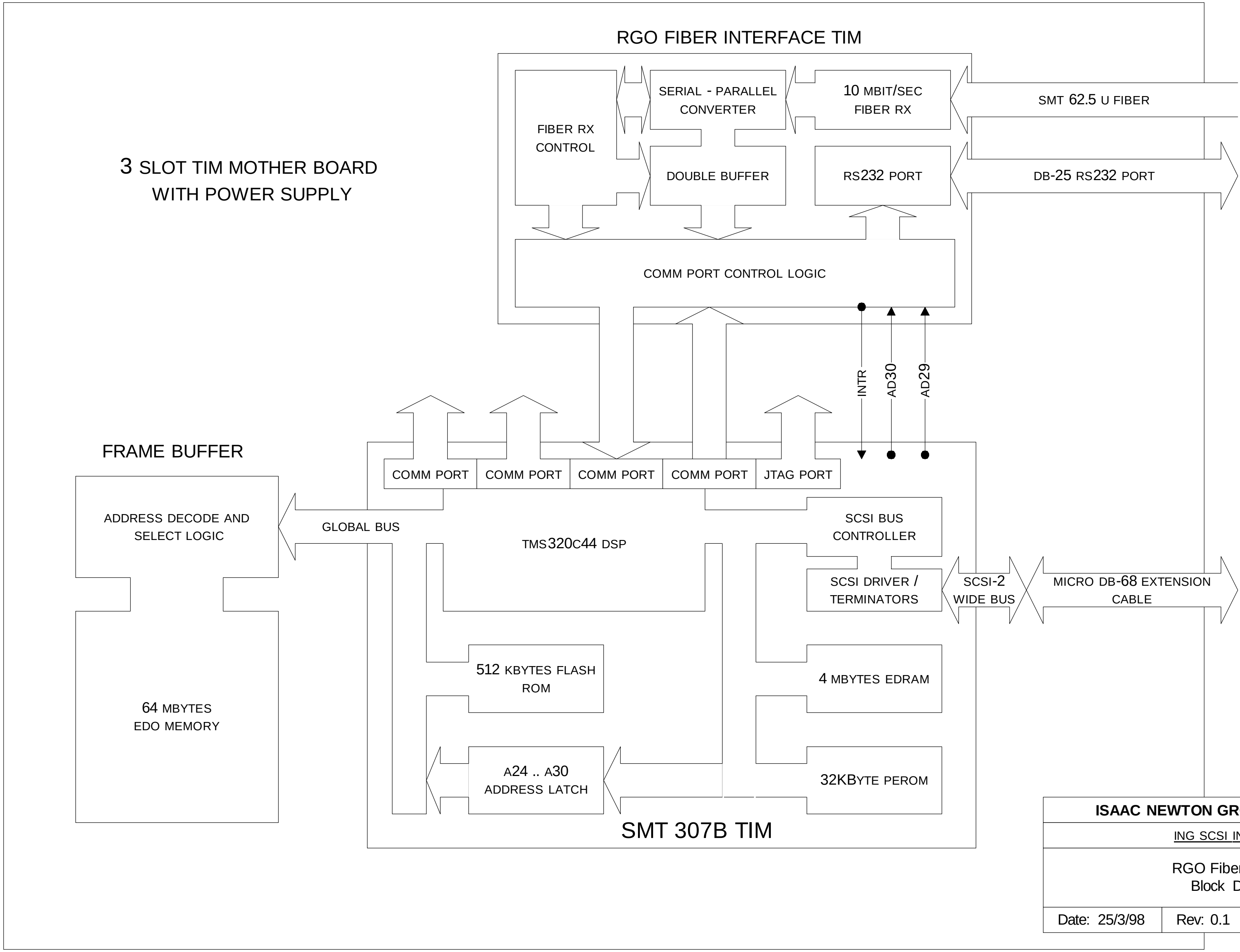
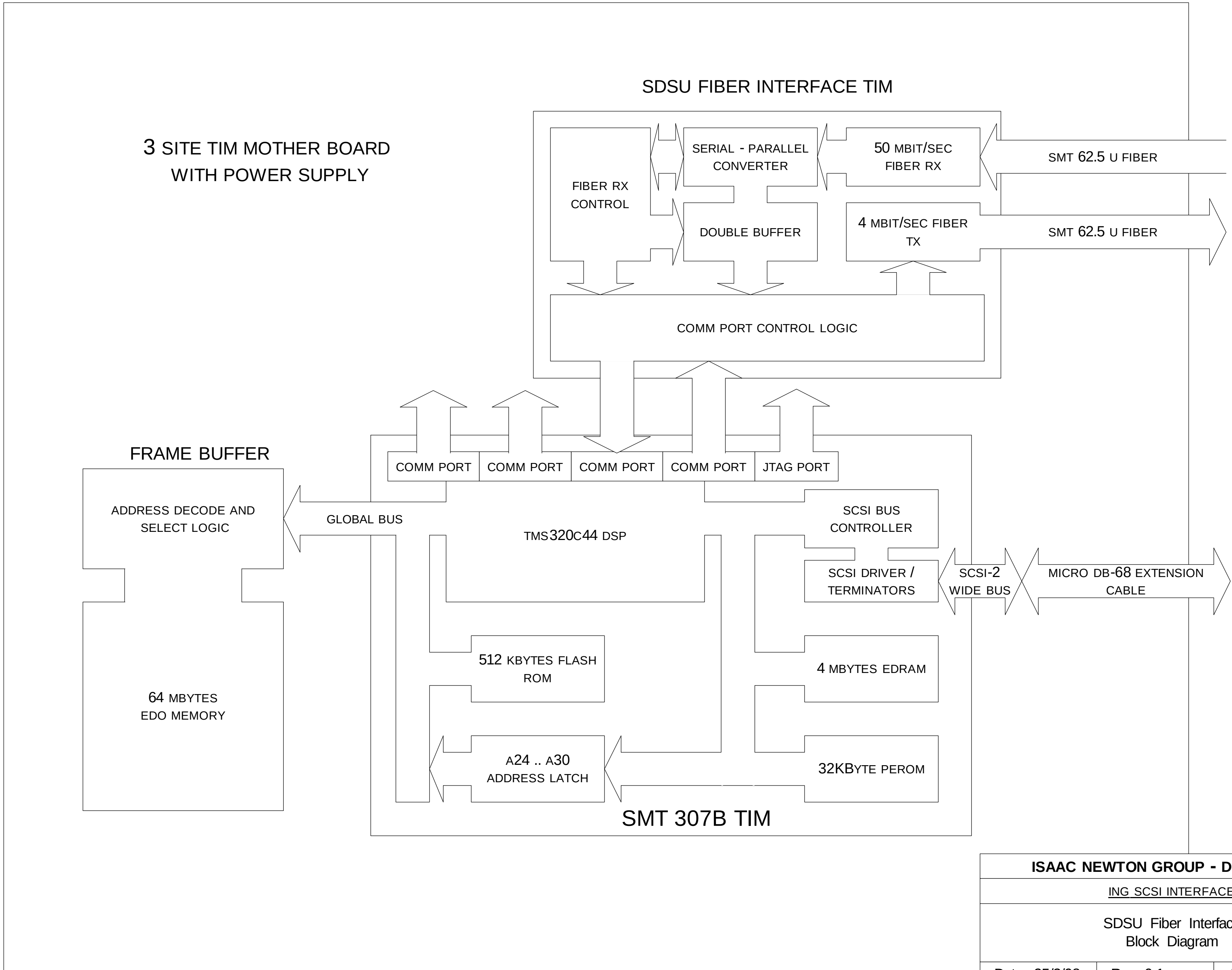


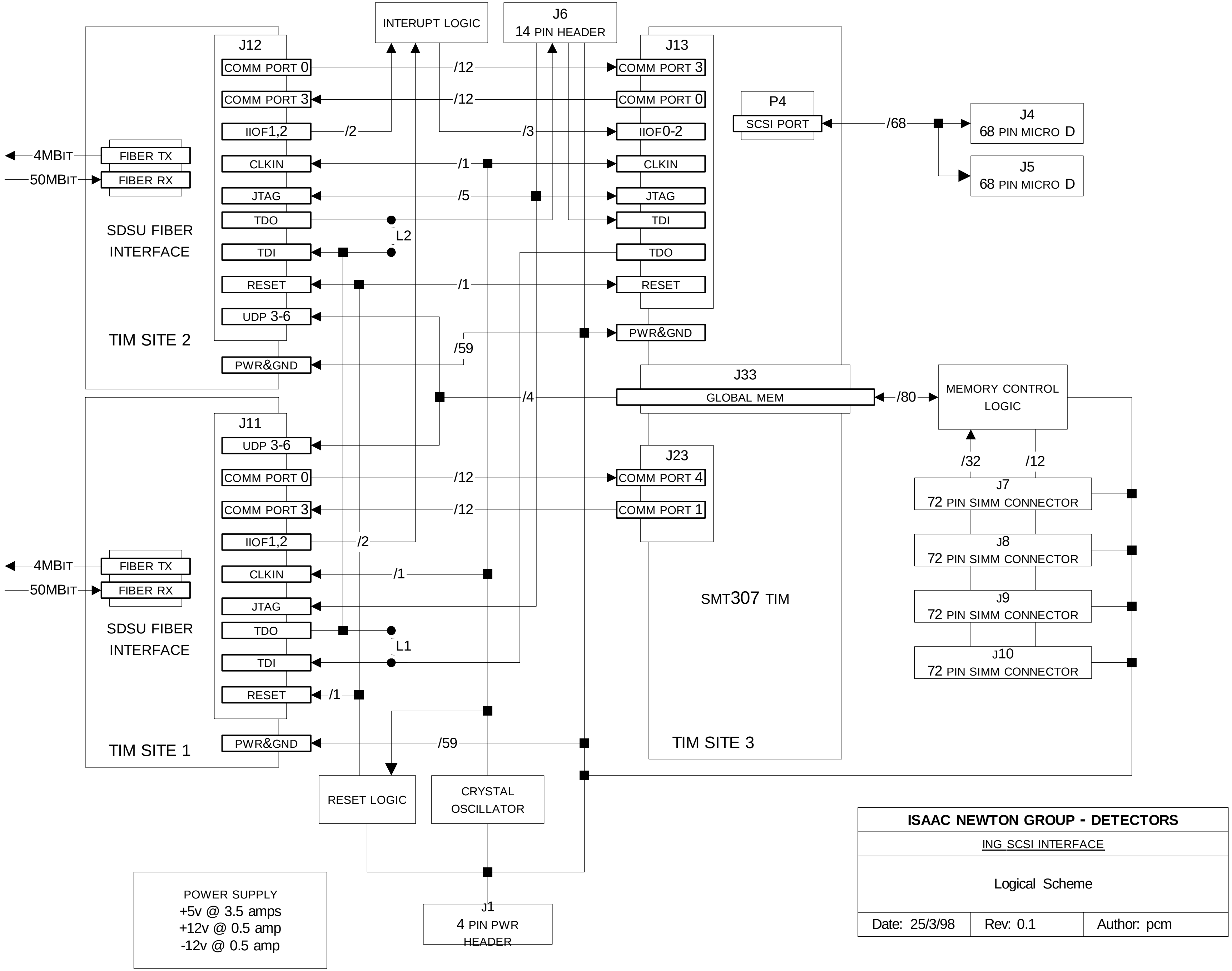
ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
General Arrangement		
Date: 25/3/98	Rev: 0.1	Author: pcm

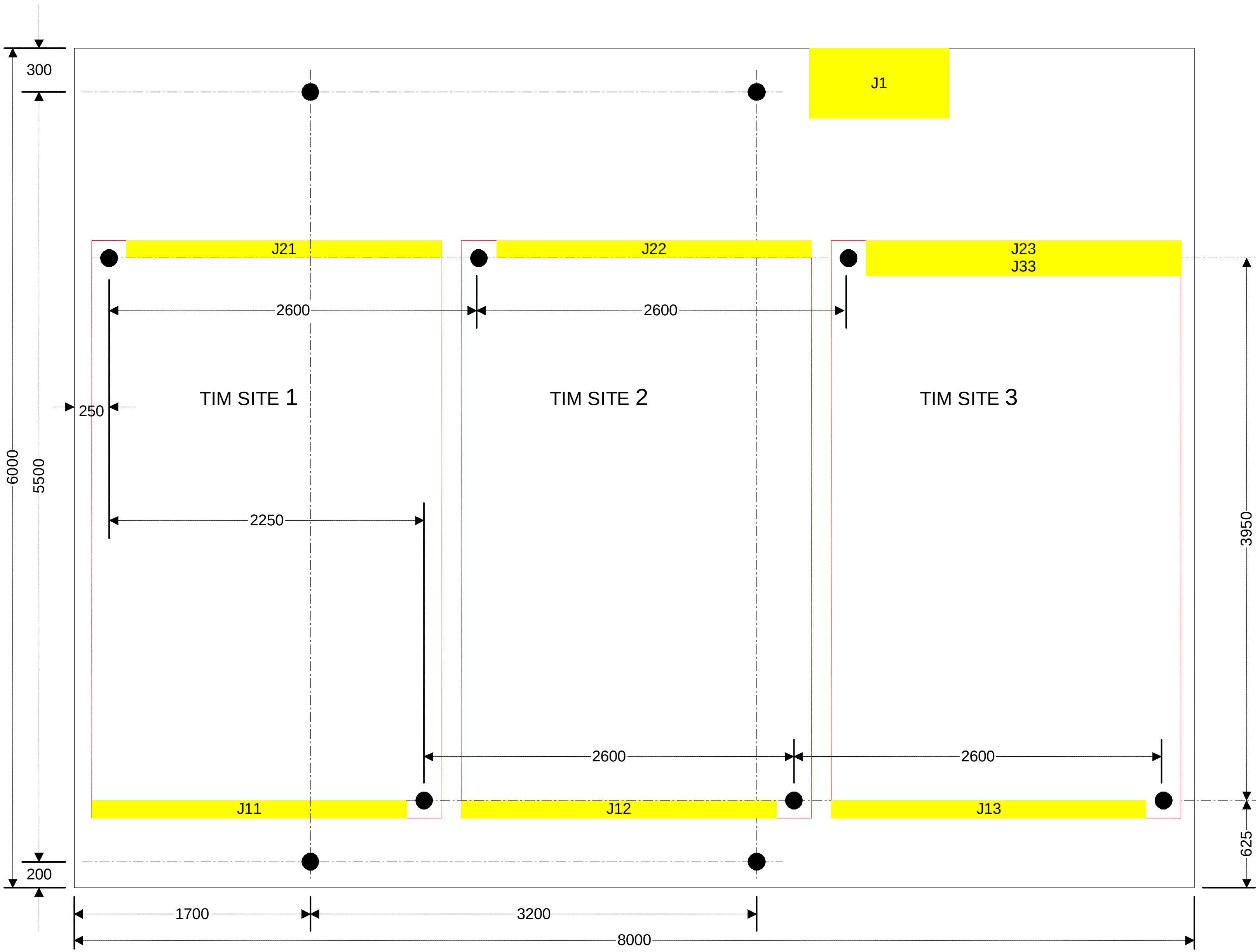


ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
RGO Fiber Interface Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm



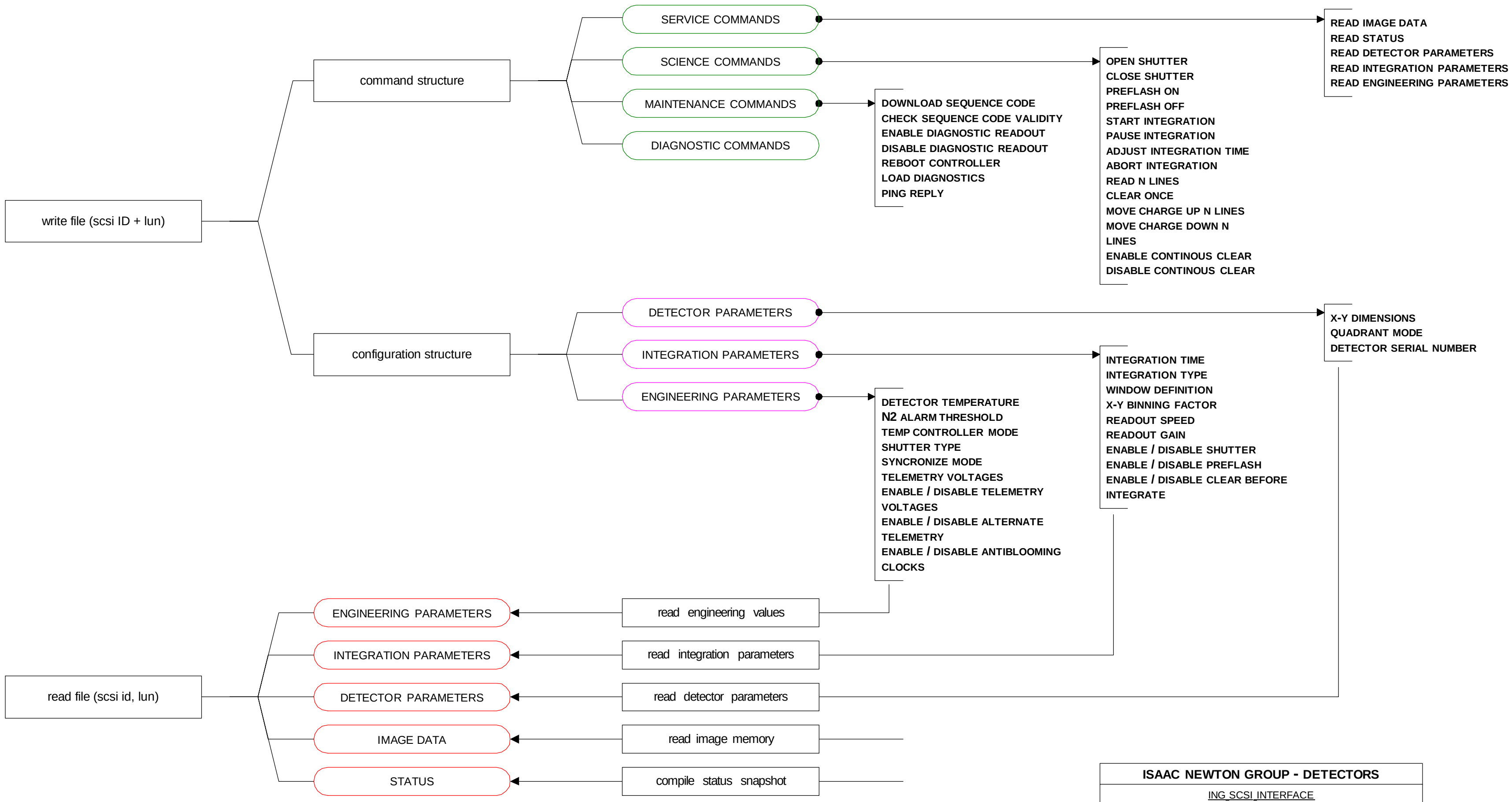
ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
SDSU Fiber Interface Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm


INTERUPT LOGIC
J6
14 PIN HEADER
J12
COMM PORT 0
COMM PORT 3
IIOF1,2
CLKIN
JTAG
TDO
TDI
RESET
UDP 3-6
PWR&GND
J13
COMM PORT 3
COMM PORT 0
IIOF0-2
CLKIN
JTAG
TDI
TDO
RESET
PWR&GND
/12
/12
/2
/3
/1
/5
L2
/1
/59
/4
4MBIT
50MBIT
FIBER TX
FIBER RX
SDSU FIBER
INTERFACE
TIM SITE 2
P4
SCSI PORT
/68
J4
68 PIN MICRO D
J5
68 PIN MICRO D
J33
GLOBAL MEM
/80
MEMORY CONTROL
LOGIC
/32
/12
J7
72 PIN SIMM CONNECTOR
J8
72 PIN SIMM CONNECTOR
J9
72 PIN SIMM CONNECTOR
J10
72 PIN SIMM CONNECTOR
J11
UDP 3-6
COMM PORT 0
COMM PORT 3
IIOF1,2
CLKIN
JTAG
TDO
TDI
RESET
PWR&GND
/12
/12
/2
/1
L1
/1
/59
J23
COMM PORT 4
COMM PORT 1
SMT307 TIM
TIM SITE 3
4MBIT
50MBIT
FIBER TX
FIBER RX
SDSU FIBER
INTERFACE
TIM SITE 1
RESET LOGIC
CRYSTAL
OSCILLATOR
J1
4 PIN PWR
HEADER
POWER SUPPLY
+5v @ 3.5 amps
+12v @ 0.5 amp
-12v @ 0.5 amp
ISAAC NEWTON GROUP - DETECTORS
ING SCSI INTERFACE
Logical Scheme
Date: 25/3/98
Rev: 0.1
Author: pcm



all dimensions in thou's
of an inch

ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
Mother Board Mechanical Layout		
Date: 25/3/98	Rev: 0.1	Author: pcm

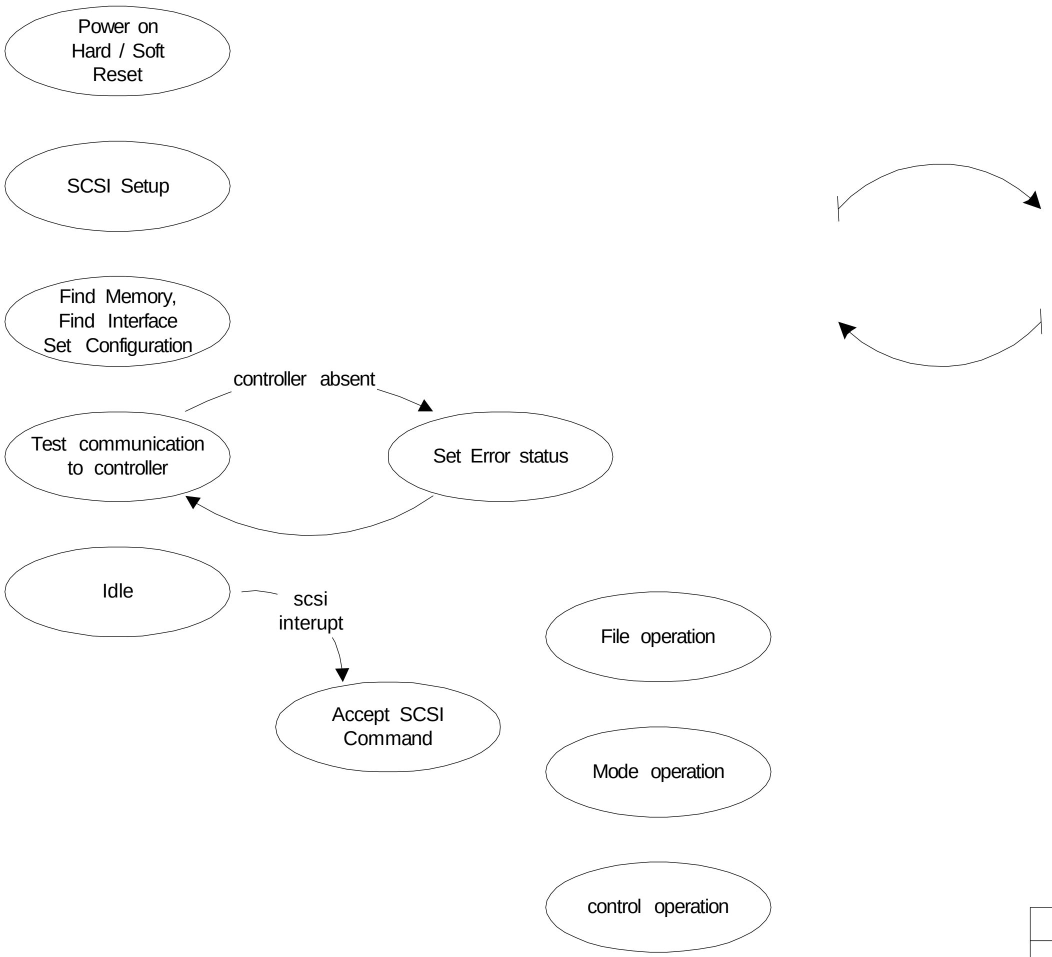


ISAAC NEWTON GROUP - DETECTORS

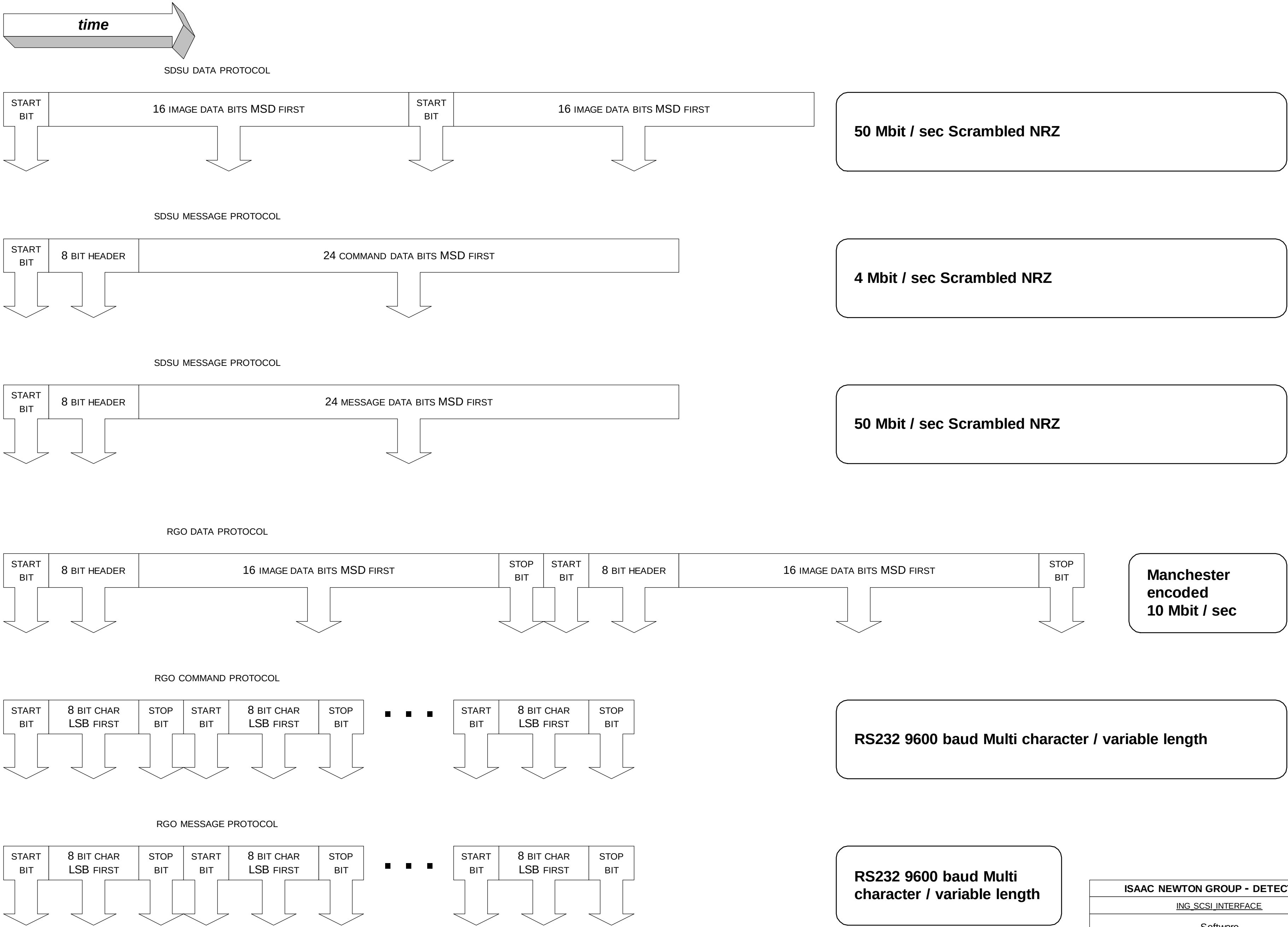
ING SCSI INTERFACE

Software
Command Set and Hierarchy

Date: 25/3/98 | Rev: 0.1 | Author: pcm



ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Software Logical Structure		
Date: 25/3/98	Rev: 0.1	Author: pcm

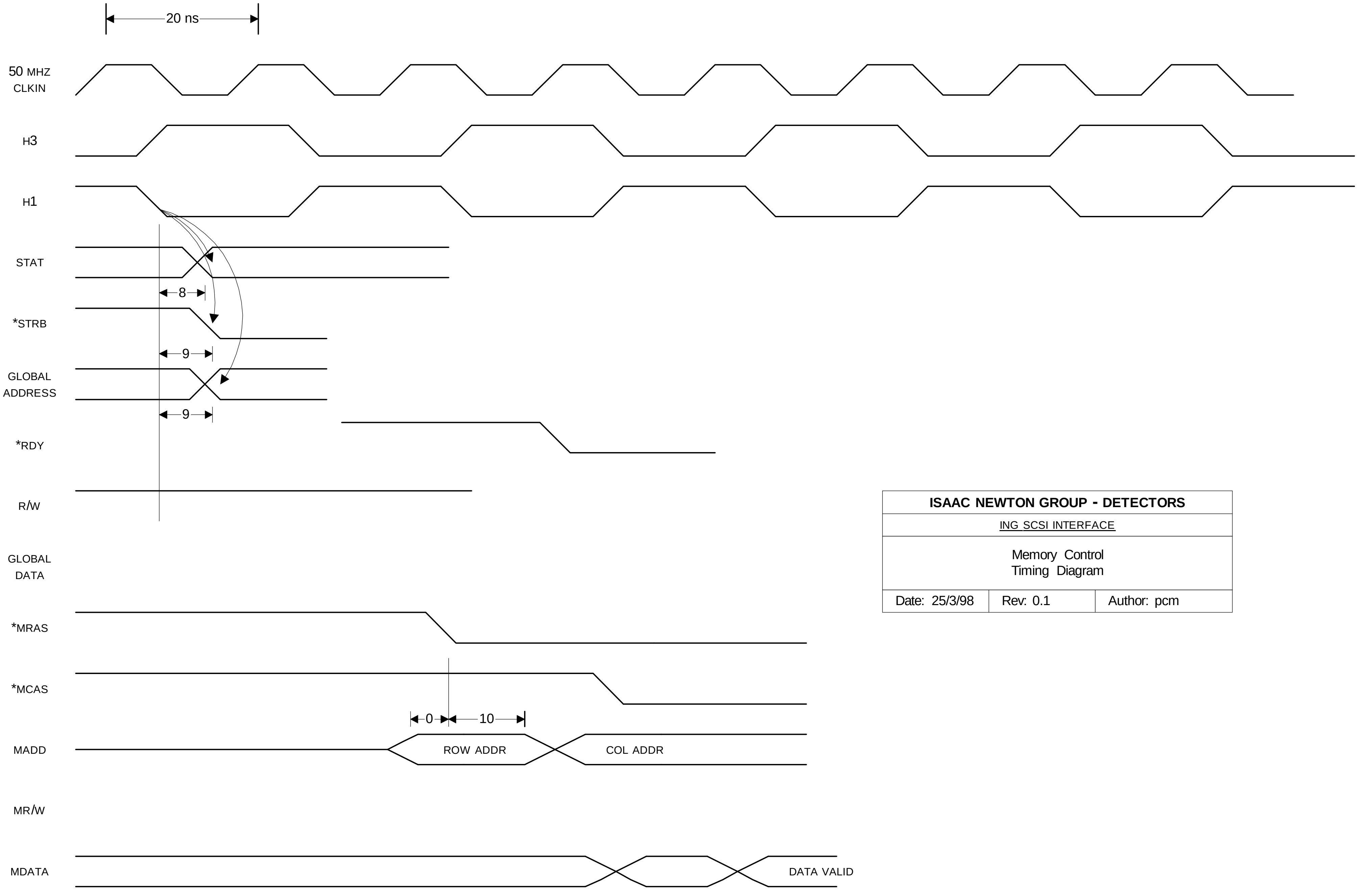


ISAAC NEWTON GROUP - DETECTORS

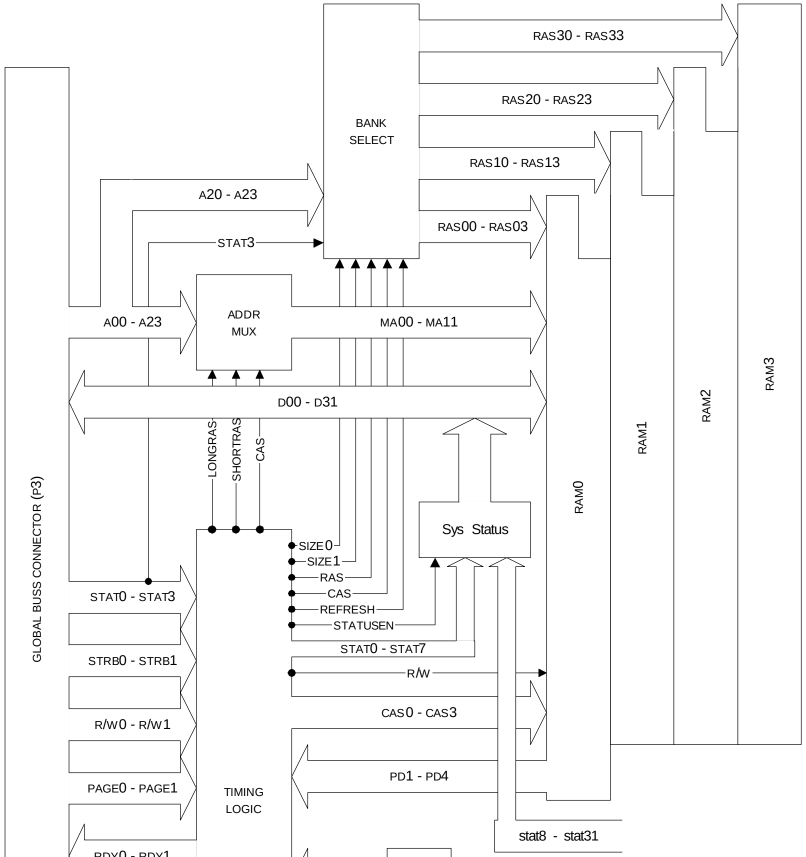
ING SCSI INTERFACE

Software
Fiber Protocols

Date: 25/3/98	Rev: 0.1	Author: pcm



ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Memory Control Timing Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm



NOTES:

1. ALL RAM MODULES MUST BE THE SAME SIZE AND SPEED.

2. MAX RAM CAPACITY = 128MBYTES USING 4 X 32MBYTE (8MB X 32) SIMMS.

3. ACCOMODATES EDO NON PARITY 2Mx32, 4Mx32, 8Mx32 5 VOLT SIMMS.

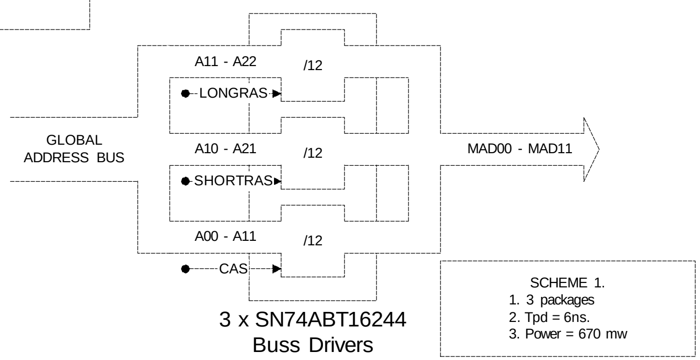
4. LOCK SIGNAL IS USED BY SOFTWARE REFRESH ACCESS

5. A24 ENABLES MEMORY BANK WHEN 8Mx32 SIMMS USED

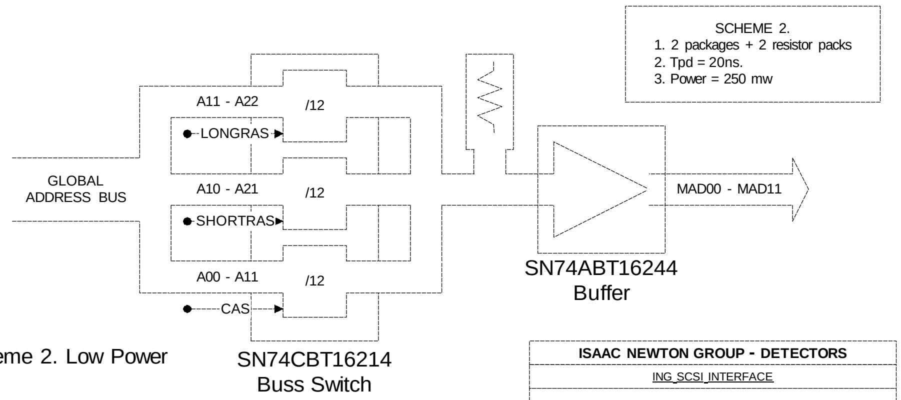
ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Memory Control Logic Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm

SIZE MBYTE	ADDRESS SPACE	32MBit SIMM	16MBit SIMM	8MBit SIMM
8	8000000 - 81FFFFF	J7	J7	J7
16	8200000 - 83FFFFF			J8
24	8400000 - 85FFFFF		J8	J9
32	8600000 - 87FFFFF			J10
40	8800000 - 89FFFFF	J8	J9	
48	8A00000 - 8BFFFFF			
56	8C00000 - 8DFFFFF		J10	
64	8E00000 - 8FFFFFF			
72	9000000 - 91FFFFF	J9		
80	9200000 - 93FFFFF			
88	9400000 - 95FFFFF			
96	9600000 - 97FFFFF			
104	9800000 - 99FFFFF	J10		
112	9A00000 - 9BFFFFF			
120	9C00000 - 9DFFFFF			
128	9E00000 - 9FFFFFF			

Scheme 1. High Speed



Scheme 2. Low Power



ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Memory Control Logic Address Mux		
Date: 25/3/98	Rev: 0.1	Author: pcm

RAS00

ISAAC NEWTON GROUP - DETECTORS
ING SCSI INTERFACE
Memory Control Logic Address Decode

Date: 25/3/98	Rev: 0.1	Author: pcm