GLOBAL MEMORY ADDRESS DECODE SCHEME

SIMM ORGANIZATION	SIMM SITES	MEMORY SIZE	ADDRESS RANGE	STRB0 PAGESIZE	STRB1 PAGESIZE	STRBACTIVE	PD1	PD2	SW0	SW1
4 x 32 MBit	J7, 8, 9, 10	128 Mbyte !	(80)000000 - (81)FFFFFF	10101	10101	10111	1	0	1	1
3 x 32 MBit	J7, 8, 9	96 Mbyte !	(80)000000 - (81)7FFFFF	10101	10101	10111	1	0	0	1
2 x 32 MBit	J7, 8	64 Mbyte !	(80)000000 - (80)FFFFFF	10101	00111	10111	1	0	1	0
1 x 32 MBit	J7	32 Mbyte !	(80)000000 - (80)7FFFFF	10101	00111	10111	1	0	0	0
4 x 16 MBit	J7, 8, 9, 10	60 Mbyte *	(80)100000 - (80)FFFFFF	01000	10101	10110	0	1	1	1
3 x 16 MBit	J7, 8, 9	44 Mbyte *	(80)100000 - (80)BFFFFF	01000	10101	10110	0	1	0	1
2 x 16 MBit	J7, 8	28 Mbyte *	(80)100000 - (80)7FFFFF	01000	10101	10110	0	1	1	0
1 x 16 MBit	J7	12 Mbyte *	(80)100000 - (80)3FFFFF	01000	10101	10110	0	1	0	0
4 x 8 MBit	J7, 8, 9, 10	32 MByte	(80)100000 - (80)8FFFFF	01000	10011	10011	1	1	1	1
3 x 8 MBit	J7, 8, 9	24 MByte	(80)100000 - (80)6FFFFF	01000	10011	10101	1	1	0	1
2 x 8 MBit	J7, 8	16 MByte	(80)100000 - (80)4FFFFF	01000	10011	10101	1	1	1	0
1 x 8 MBit	J7	8 MByte	(80)100000 - (80)2FFFFF	01000	10011	10101	1	1	0	0

NOTES:

! A24 must be set high through the SMT307 global expansion register to enable global memory, boot code exists in flash ram between addresses 8000000 - 8007FFFF which is enabled at reset.

* 4Mbytes of ram memory is shadowed by the boot flash rom on strobe 0

ROW ADDRESS DECODE SCHEME

PD 1	PD 2	SW 0	SW 1	RAS00	RAS01	RAS10	RAS11	RAS20	RAS21	RAS30	RAS31
				RAS02	RAS03	RAS12	RAS13	RAS22	RAS23	RAS32	RAS33
1	0	1	1	80000000	80400000	80800000	80C00000	81000000	81400000	81800000	81C00000
				803FFFFF	807FFFFF	80BFFFFF	80FFFFFF	813FFFFF	817FFFFF	81BFFFFF	81FFFFFF
1	0	0	1	80000000	80400000	80800000	80C00000	81000000	81400000		
				803FFFFF	807FFFFF	80BFFFFF	80FFFFFF	813FFFFF	817FFFFF		
1	0	1	0	80000000	80400000	80800000	80C00000				
				803FFFFF	807FFFFF	80BFFFFF	80FFFFFF				
1	0	0	0	80000000	80400000						
				803FFFFF	807FFFFF						
0	1	1	1	80100000		80400000		80800000		80C00000	
				803FFFFF		807FFFFF		80BFFFFF		80FFFFFF	
0	1	0	1	80100000		80400000		80800000			
				803FFFFF		807FFFFF		80BFFFFF			
0	1	1	0	80100000		80400000					
				803FFFFF		807FFFFF					
0	1	0	0	80100000							
				803FFFFF							
1	1	1	1	80100000	80200000	80300000	80400000	80500000	80600000	80700000	80800000
				801FFFFF	802FFFFF	803FFFFF	804FFFFF	805FFFFF	807FFFFF	807FFFFF	808FFFFF
1	1	0	1	80100000	80200000	80300000	80400000	80500000	80600000		
				801FFFFF	802FFFFF	803FFFFF	804FFFFF	805FFFFF	807FFFFF		
1	1	1	0	80100000	80200000	80300000	80400000				
				801FFFFF	802FFFFF	803FFFFF	804FFFFF				
1	1	0	0	80100000	80200000						
				801FFFFF	802FFFFF						

ADDRESS DECODE TRUTH TABLE

LOGIC INPUTS									LOGIC OUTPUTS							
SIZE0	**SIZE1**	**/REFRESH**	**/RAS**	**STAT3**	**A20**	**A21**	**A22**	**A23**	**/RAS00**	**/RAS01**	**/RAS10**	**/RAS11**	**/RAS20**	**/RAS21**	**/RAS30**	**/RAS31**
x	x	x	1	x	x	x	x	x	1	1	1	1	1	1	1	1
x	x	0	0	x	x	x	x	x	0	0	0	0	0	0	0	0
1	0	1	0	0	x	x	0	0	0	1	1	1	1	1	1	1
1	0	1	0	0	x	x	1	0	1	0	1	1	1	1	1	1
1	0	1	0	0	x	x	0	1	1	1	0	1	1	1	1	1
1	0	1	0	0	x	x	1	1	1	1	1	0	1	1	1	1
1	0	1	0	1	x	x	0	0	1	1	1	1	0	1	1	1
1	0	1	0	1	x	x	1	0	1	1	1	1	1	0	1	1
1	0	1	0	1	x	x	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	x	x	1	1	1	1	1	1	1	1	1	0
0	1	1	0	1	x	x	0	0	0	1	1	1	1	1	1	1
0	1	1	0	1	x	x	1	0	1	1	0	1	1	1	1	1
0	1	1	0	1	x	x	0	1	1	1	1	1	0	1	1	1
0	1	1	0	1	x	x	1	1	1	1	1	1	1	1	0	1
1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
1	1	1	0	1	0	1	0	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	1
1	1	1	0	1	0	0	1	0	1	1	1	0	1	1	1	1
1	1	1	0	1	1	0	1	0	1	1	1	1	0	1	1	1
1	1	1	0	1	0	1	1	0	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	0	1	0	0	0	1	1	1	1	1	1	1	1	0

DECODE LOGIC ALGORITHM

MEMORY ADDRESS MUX CODING

	SHORTRAS		LONGRAS	
ADDR	**RAS**	**CAS**	**RAS**	**CAS**
MA00	A10	A00	A11	A00
MA01	A11	A01	A12	A01
MA02	A12	A02	A13	A02
MA03	A13	A03	A14	A03
MA04	A14	A04	A15	A04
MA05	A15	A05	A16	A05
MA06	A16	A06	A17	A06
MA07	A17	A07	A18	A07
MA08	A18	A08	A19	A08
MA09	A19	A09	A20	A09
MA10	A20	A10	A21	A10
MA11	A21	A11	A22	A11

U2 PIN ASSIGNMENTS (PALCE20V10)

PIN #	DES	SIG	I/O	NOTES
	I0	GAD20	I	ADDRESS 20
	I1	GAD21	I	ADDRESS 21
	I2	GAD22	I	ADDRESS 22
	I3	GAD23	I	ADDRESS 23
	I4	STAT3	I	STROBE 0/1
	I5			NOT CONNECTED
	I6	/REFRESH	I	FROM U6
	I7	/64RAS	I	FROM U6
	I8	/32RAS	I	FROM U6
	I9	/8RAS	I	FROM U6
	I/O0	/RAS00	O	J7 LOWER ROW SELECT
	I/O1	/RAS01	O	J7 UPPER ROW SELECT
	I/O2	/RAS10	O	J8 LOWER ROW SELECT
	I/O3	/RAS11	O	J8 UPPER ROW SELECT
	I/O4	/RAS20	O	J9 LOWER ROW SELECT
	I/O5	/RAS21	O	J9 UPPER ROW SELECT
	I/O6	/RAS30	O	J10 LOWER ROW SELECT
	I/O7	/RAS31	O	J10 UPPER ROW SELECT
	I/O8	PD1	I	
	I/O9	PD2	I	

U6 PIN DEFINITIONS (MACH 210)

PIN #	DES	SIG	I/O	NOTES
	IN0	50CLK	I	50 Mhz BASIC CLOCK
	IN1	/STRB0	I	TIM40 MEMORY BANK 0 STROBE
	IN2	/STRB1	I	TIM40 MEMORY BANK 1 STROBE
	IN3	H3CLK	I	TIM40 25Mhz CLOCK
	IN4		I	
	IN5		I	
	I/O0	PAGE0	I	
	I/O1	RNWD0	I	
	I/O2	RDY0	O	
	I/O3	PAG1	I	
	I/O4	RNWD1	I	
	I/O5	RDY1	O	
	I/O6			
	I/O7			
	I/O8	/CONFIG	I	
	I/O9	/RESET	O	RESET GENERATOR OUTPUT
	I/O10	/WE	O	WRITE ENABLE TO RAM BANKS
	I/O11	/CAS0	O	COMMON CAS STROBE TO RAM BANKS
	I/O12	/CAS1	O	COMMON CAS STROBE TO RAM BANKS
	I/O13	STAT3	I	TIM40 MEMORY ACCESS STATUS NIBBLE
	I/O14	STAT2	I	
	I/O15	STAT1	I	
	I/O16	STAT0	I	
	I/O17	LOCK	I	TIM40 MEMORY LOCK, USED TO DETERMINE REFRESH CYCLE
	I/O18	/REFRESH	O	
	I/O19	/64RAS	O	
	I/O20	/32RAS	O	
	I/O21	/8RAS	O	
	I/O22	PD4	I	
	I/O23	PD3	I	
	I/O24	PD2	I	
	I/O25	PD1	I	

I/O26	/STATUS	O	
I/O27			
I/O28	ENBL0	O	CAS ADDRESS ENABLE
I/O29	ENBL1	O	8MBIT RAS ADDRESS ENABLE
I/O30	ENBL2	O	32MBIT RAS ADDRESS ENABLE
I/O31	ENBL3	O	64MBIT RAS ADDRESS ENABLE