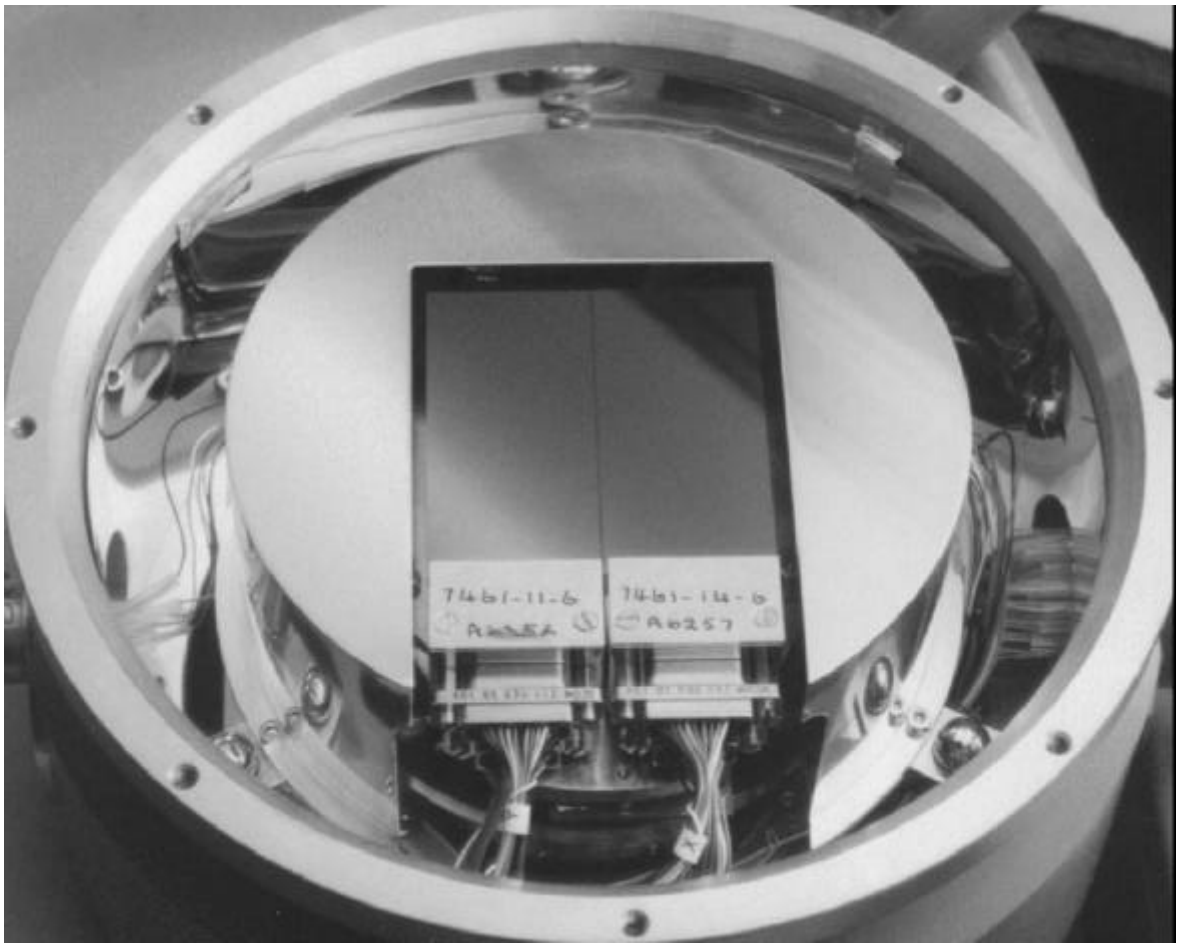
ING Technical Note 119
The 2 Chip EEV Mosaic

Simon Tulloch. November 1998



CONTENTS

1. General Description.

The camera contains two EEV-42-80 thinned and AR coated CCDs butted along their long axes to provide a 4K x 4K pixel mosaic. 13.5μm pixels. 2148 x 4128 pixels total including 50 x-underscan, 50 x-overscan and 28 y-overscan pixels. The active area of the mosaic measures 55.8 x 55.35 mm, with a 0.53mm gap between the chips. Both chips have two working amplifiers giving 3 - 4 electrons noise.

CCD 1 Device number : 7461-14-6.
Grade 2 device with six bright columns and one dark Bright defects :600 total, 230 in central zone. QE = 62% at 380nm, 78% at 400nm, 75% at 650nm and 14% at 950nm.
No measurable dark current at –120C. Full well 170,000 electrons.

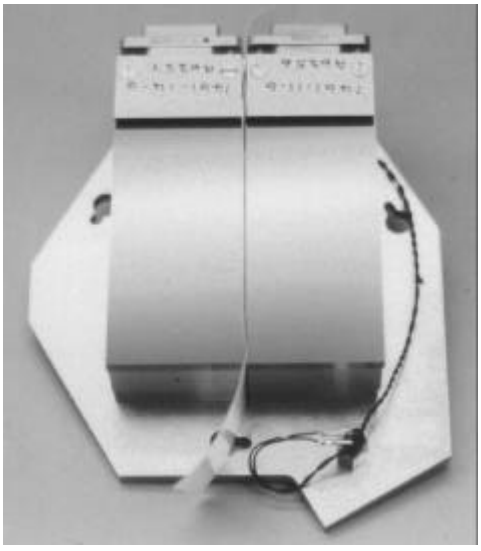
CCD 2 Device number : 7461-11-6.
Grade 1 device with one bright column . Bright defects 55 total, 16 in central zone.
QE = 67% at 380nm, 81% at 400nm, 76% at 650nm and 13% at 950nm.
No measurable dark current at –120C. Full well 210,000 electrons.

These two devices come from a production run that resulted in an elevated channel potential . There operational voltages are different from normal EEV42-80s.

The camera was characterised using a Dutch controller configured for two channel readout. It used two Clock cards, two ADC cards , two CDS cards and two Fibre cards. A custom designed two channel preamplifier was also used. Details of the controller configuration are included in this report.

All test data was recorded at -120C.

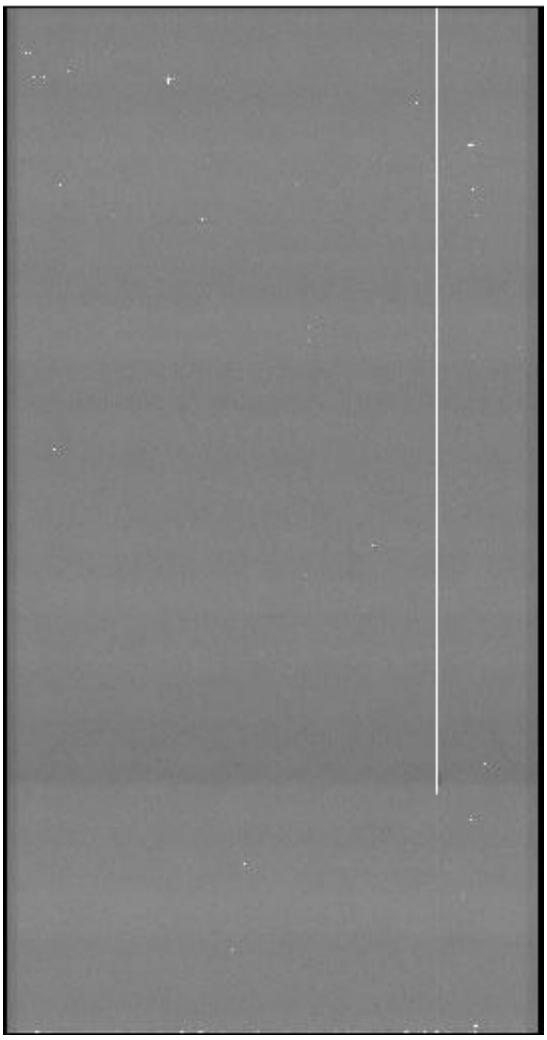
The mosaic during assembly



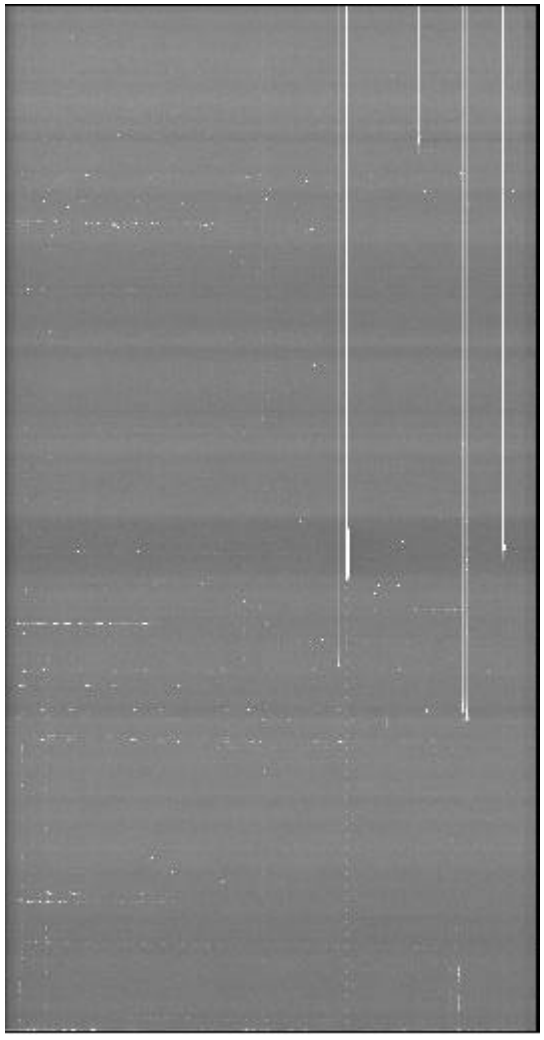
2. Image Quality

2.1. Image Defects.

The following images are each the result of stacking five 900s dark frames using an algorithm to reject cosmic rays. They show hot spots and defective columns.



Chip 2 (7461-11-6)

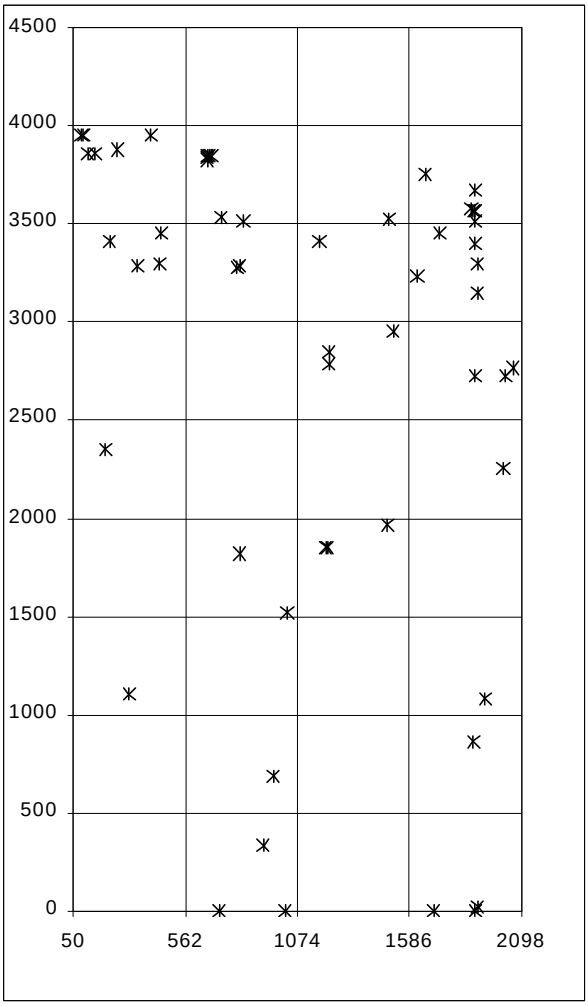


Chip 1 (7461-14-6)

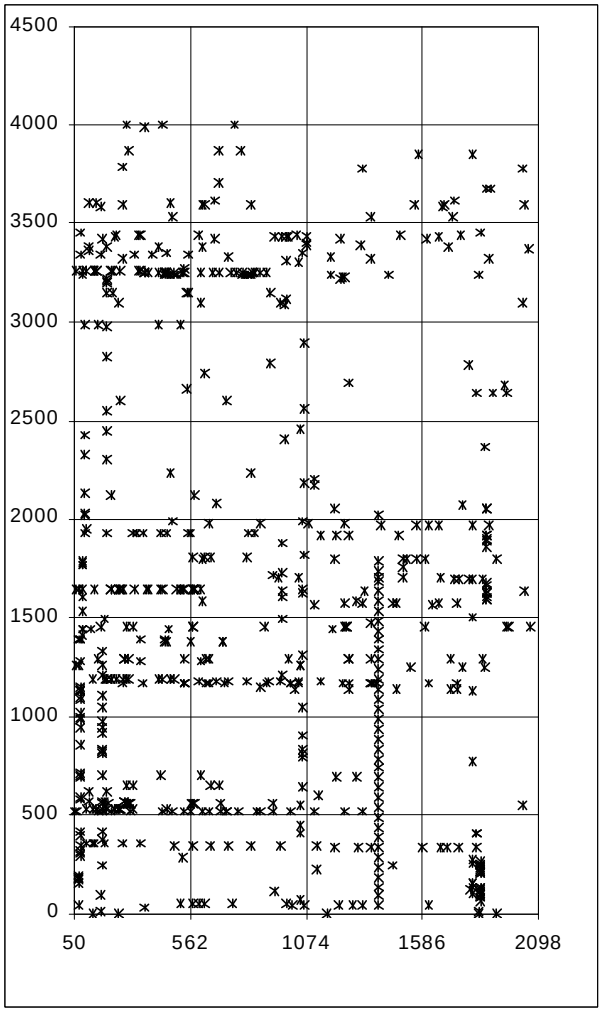
Both Images taken with left hand amplifier

Mosaic Chip	Bright Columns locations	Dark Columns locations	Number of Hot Spots
CCD1	1391,1359,1676, 1852,1870,2016	2001	634
CCD2	1740	none	55

Hot Pixel Maps :-



Chip 2



Chip 1

Both images taken through left-hand amplifiers.

The cosmic ray count was surprisingly different for the two chips; chip 1 gave 4300 events per hour, chip 2 gave 2500 events per hour.

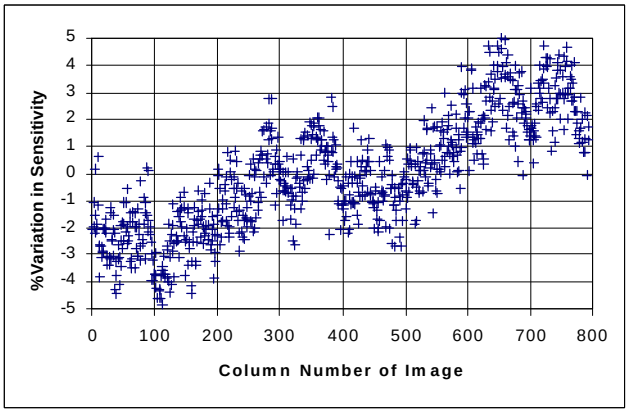
2.2. Pixel Response Non-Uniformity.

This was measured using deeply exposed flat-fields and taking a cut across each image. There was some uneveness in the illumination but the pixel to pixel sensitivity variations

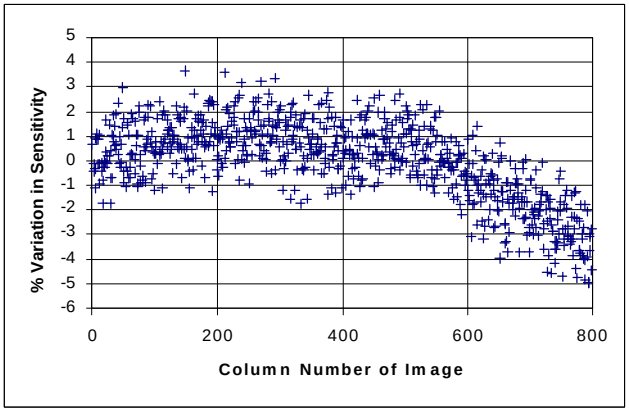
are clearly visible. At 390nm a cross hatch pattern with a spatial period of about 350 pixels is visible. If the chips were illuminated at 950nm with a collimated source, fringes with an amplitude of 13 % were also visible.

Mosaic CCD 1 :-

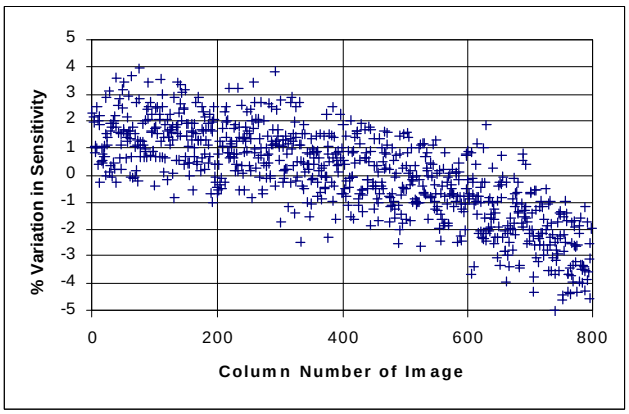
390nm.



565nm.

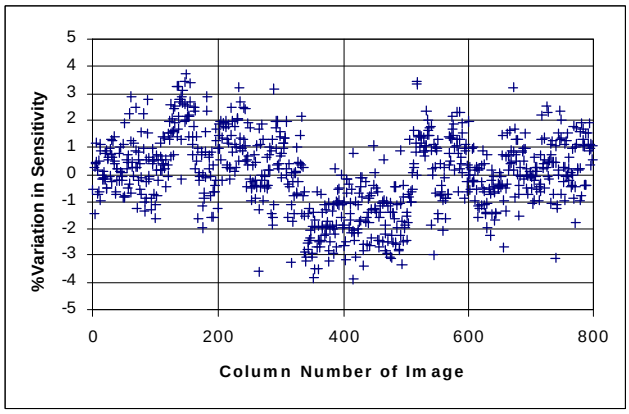


950nm

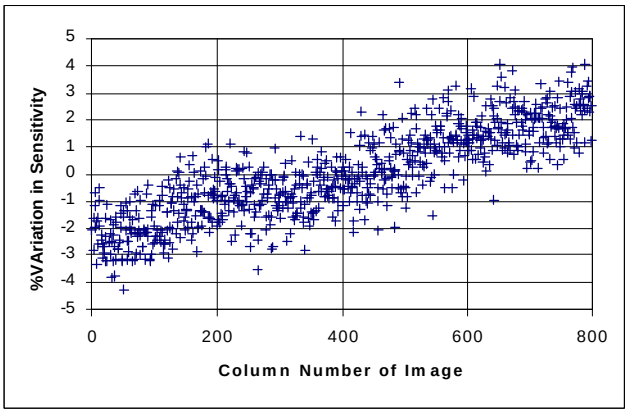


Mosaic CCD 2 :-

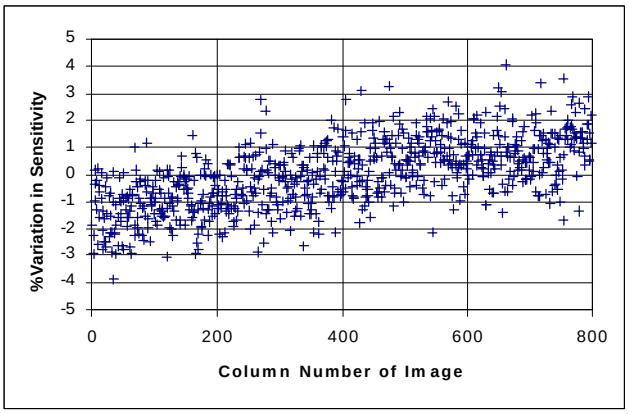
390nm.



565nm.



950nm



3. Read Out Noise.

The readout noise was characterised for all outputs in both hi-gain and lo-gain mode. These modes were selected by switching the voltage on OG2 so as to vary the output node capacitance.

The output sensitivities of the CCDs are shown below in μV/electron.

CCD	Left Output Hi-gain Sensitivity	Right Output Hi-gain Sensitivity	Left Output Lo-gain Sensitivity	Right Output Lo-gain Sensitivity
1	2.95	3.3	1.1	1.1
2	2.8	4.15	1.2	1.4

The RMS noise is tabulated below for a variety of CDS integration times. In all cases the CDS RC constant was 4.3μs. Both CCDs gave significantly higher gain and lower noise with their right hand outputs.

CCD 1 in Hi-Gain	8+8μs CDS time	6+6μs CDS time	4+4μs CDS time
Left Output	4.1e	3.8e	5.2e
Right Output	3.3e	3.5e	3.5e

CCD 2 in Hi-Gain	8+8μs CDS time	6+6μs CDS time	4+4μs CDS time
Left Output	4.4e	4.9e	6.2e
Right Output	3.2e	3.5e	4.1e

CCD 1 in Lo-Gain	8+8μs CDS time	6+6μs CDS time	4+4μs CDS time
Left Output	9.8e		10.5e
Right Output			8.6e

CCD 2 in Lo-Gain	8+8μs CDS time	6+6μs CDS time	4+4μs CDS time
Left Output	10.0		13.2e
Right Output			10e

Noise and gain are critically dependent on the operational voltages. In particular the output FET drain and image area clock- low should be set to within 100mV of the voltages recommended in Appendix A.

4. Charge Transfer Efficiency

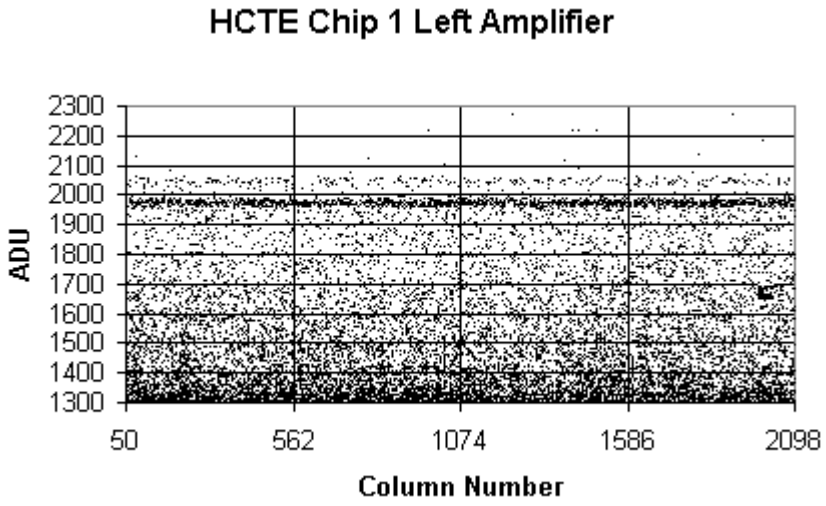
Measured using extended pixel edge response for chip 1 . Lo-Level corresponds to a signal charge of 1600 electrons, Hi-Level to a signal level of 100,000 electrons

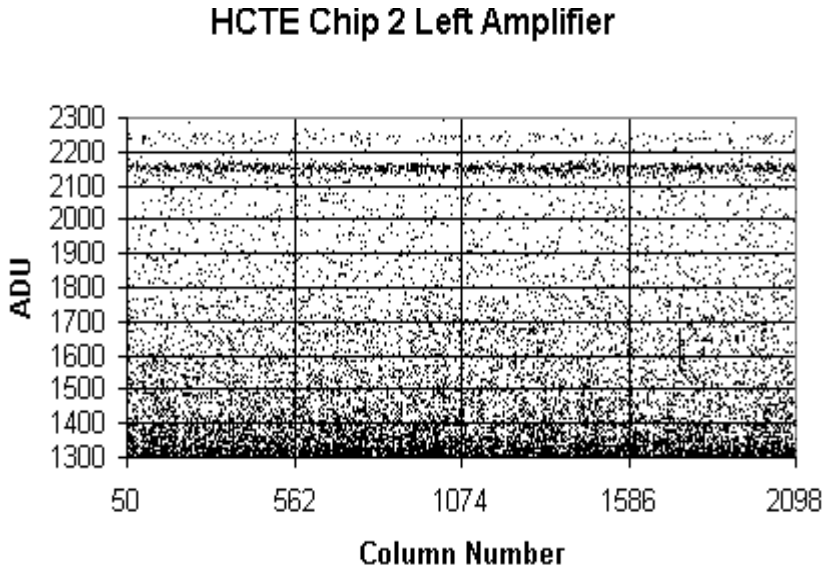
CCD 1	VCTE Lo-Level	VCTE Hi-Level	HCTE Lo-Level	HCTE Hi-Level
Left Output	0.999998	0.999997	0.999997	0.999998
Right Output	0.999998	0.999997	0.999997	0.999998

Chip 2 was measured using the Fe-55 X-ray method:

CCD 2	HCTE Lo-Level	VCTE Lo-Level
Left Output	0.999997	>0.999999
Right Output	>0.999999	

The Fe55 x-ray plots from the left hand amplifier of each chip are shown below.



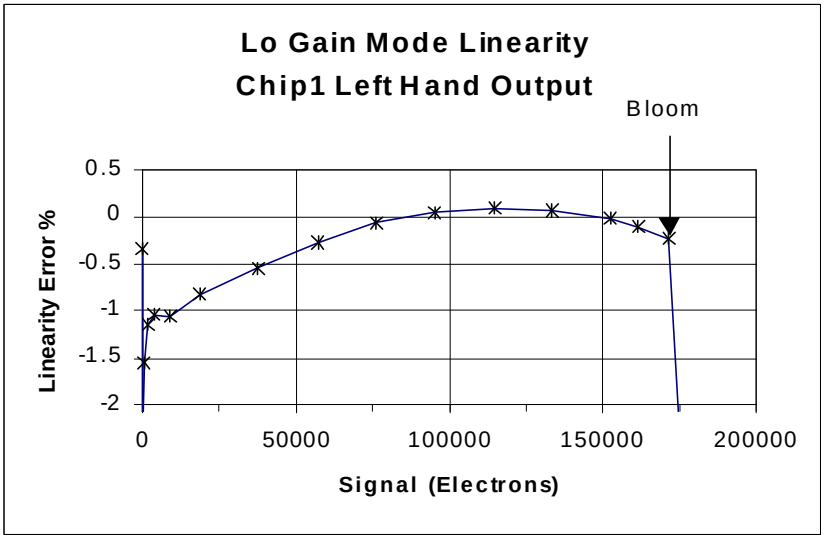


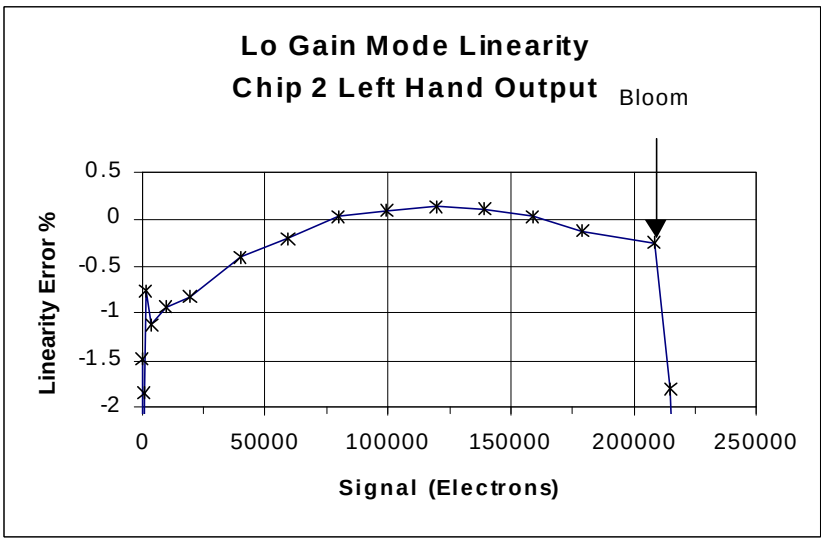
5. Full Well and Linearity

Full well was measured in Lo-gain mode using a pulsed LED source. The point at which the signal became sharply non-linear was coincident with the onset of vertical blooming in the image. High-gain linearity measurements are in agreement with EEV data sheets; chip 2, output right is exceptionally linear, chip 1 output right has very poor linearity.

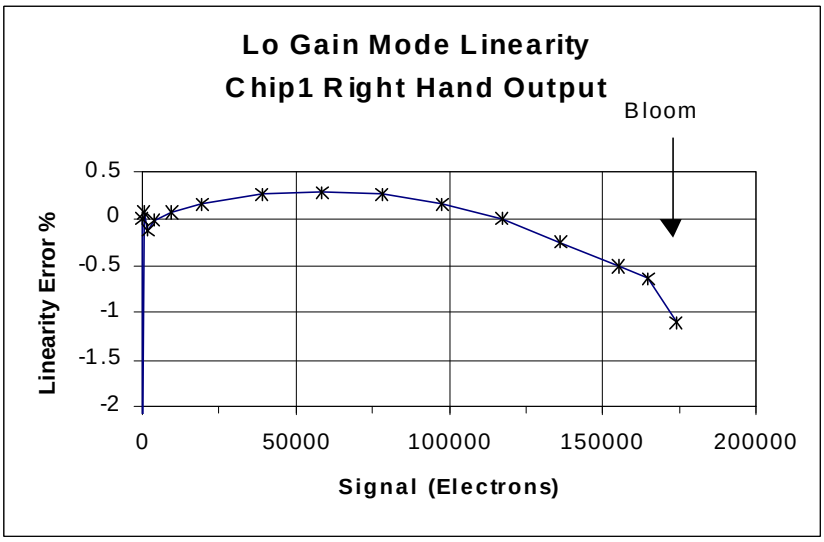
Chip 1 : Full well = 170,000 electrons
Chip 2 : Full well = 210,000 electrons

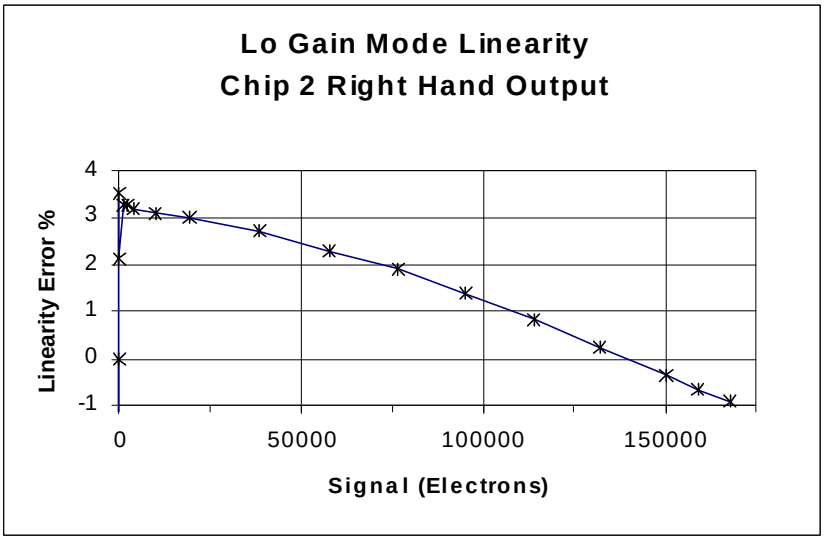
Lo-gain , left hand outputs :-



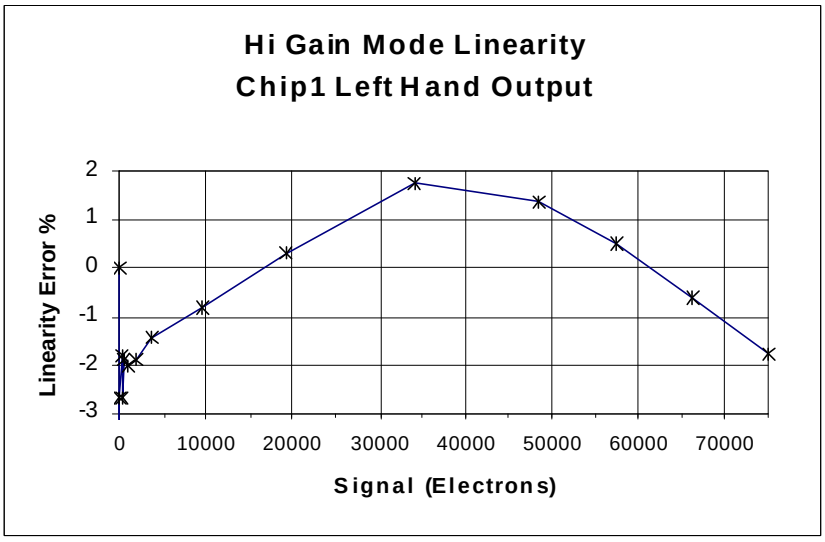


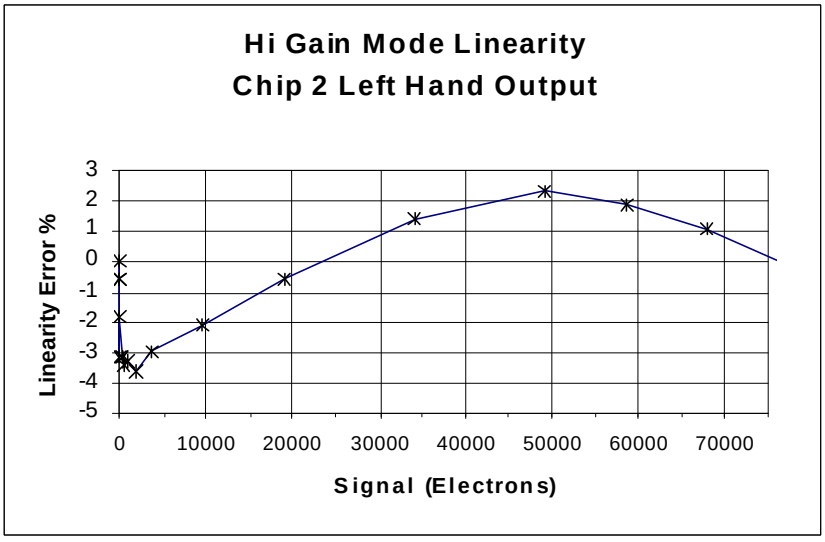
Lo-gain , right hand outputs :-



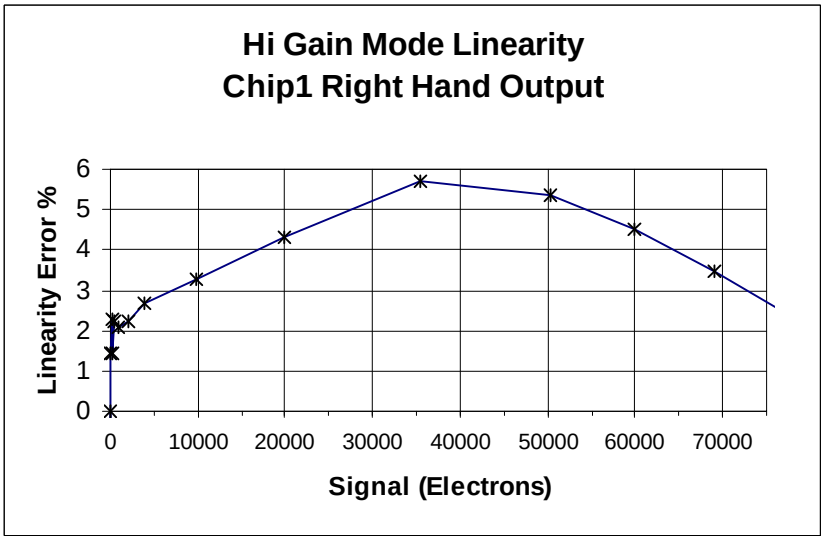


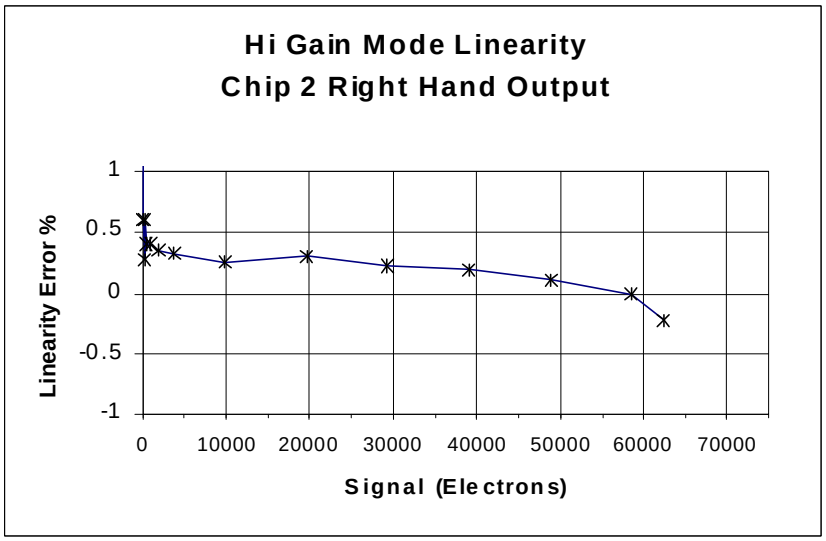
Hi-gain , left hand outputs :-





Hi-gain , right hand outputs :-





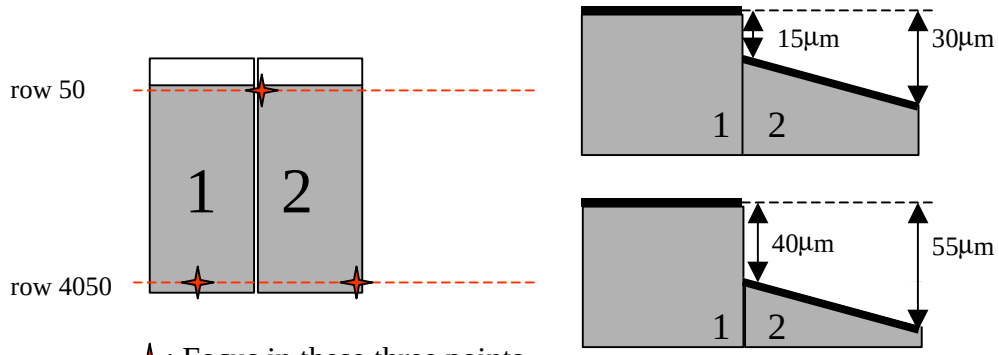
The linearity is fairly typical for EEV42-80s, although chip 2 right hand output is exceptionally good in hi-gain mode . The poor linearity of the chip 1 right hand side amplifier is mentioned on the EEV data sheet. The RD and OD voltages were varied by +/- 0.5V in effort to improve the performance , but to no effect.

6. Mechanical Parameters.

The Mosaic was built into a 2.5 l Oxford Instruments blue cryostat. The LN_2 hold time when servoing at -120°C and held horizontally, with the fill tube at 12 '0' clock position, was 19.5 hours. The heater servo power required to maintain this temperature was 200mW.

6.1. Mosaic Coplanarity and Spacing.

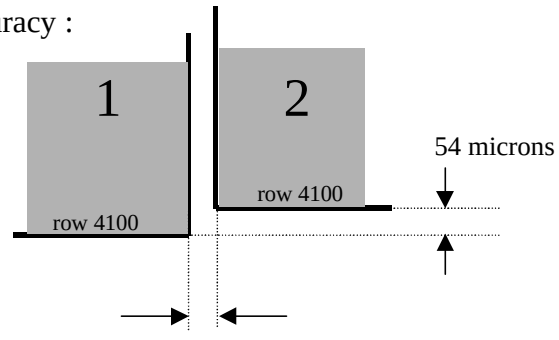
The coplanarity and relative positions of the two chips was measured using the RGO flatness scanner. Each chip was flat to within the resolution of the flatness scanner, which in this case was about 5µm.



✦: Focus in these three points
and co-planarity will be +/-20µm
Point 1 : CCD 1 : column 1150, row 4000
Point 2 : CCD 2 : column 2000, row 100
Point 3 : CCD 2 : column 100 , row 4000

Chip butting was done with the aid of 50µm PTFE shims that were removed after the chips were securely bolted to the base plate. The gap between active Silicon on either side of the join is approximately 39 pixels.

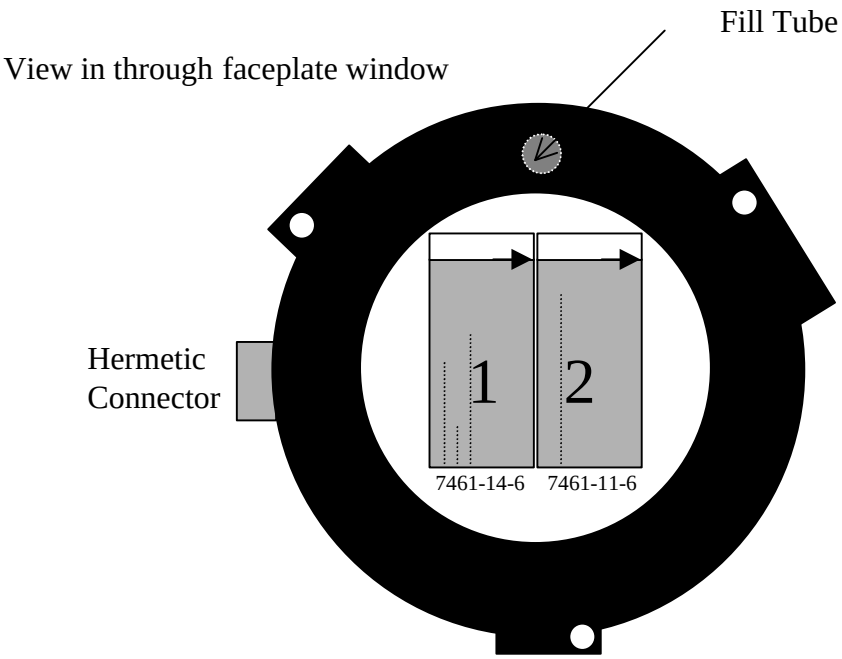
Chip Butting Accuracy :



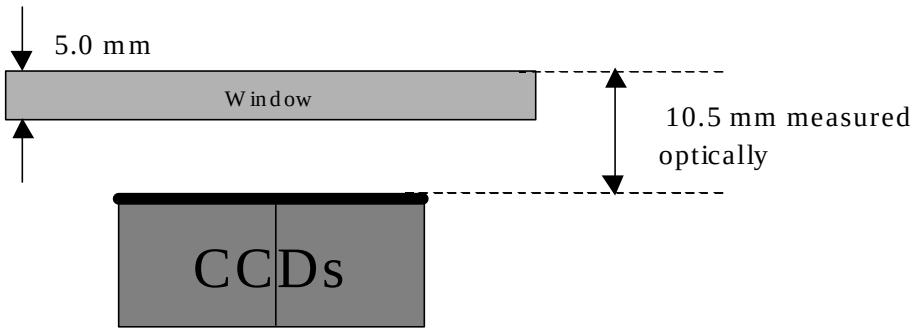
530 microns between active pixels

6.2 Mosaic Alignment within Cryostat

The orientation of the chips in the cryostat is orthogonal to a normal EEV 42-80 camera ; the long axis is parallel to the primary dispersion axis when used at UES on the William Herschel telescope.



The cryostat window had a thickness of 5mm. The distance from the front face of the window to the surface of the CCD was measured using a travelling microscope.



7. Operation with SDSU controller

There may be some problem operating the temperature servo from the SDSU controller since it is designed to use temperature sensing diodes rather than resistance thermometers. The equilibrium temperature of the mosaic in the lab, with the temperature servo disconnected, is -125 degrees C, which is only 5 degrees colder than the chosen operating temperature. Even without the temperature servo running the mosaic should still give satisfactory performance.

One of the CCDs will not image unless Serial Phase 3 is held high during transfer into the serial register.

To minimise leakage into the image area during integration hold all the serial phases , the reset clock and the dump gate high.

Appendix A. Operating Voltages

When characterised using the Dutch controller, the mosaic chips had common Substrate, OG1 and OG2 connections. All the other connections were independently driven using separate clock boards for the two chips. Cross talk between the chips was just visible on frames containing bright extended sources, but cross sections across these ghosts revealed that they had sub-ADU amplitude.

The operating voltages were measured at the pre-amp using a DVM and were identical for both CCDs.

Image Area clocks :	Lo	-16.0V
	Hi	-3.5V
Serial Register clocks:	Lo	- 14.6V
	Hi	- 3.5V
Substrate:		-6V
OG2 Lo-gain		+3V
OG2 Hi-gain		-12V
OG1		-13V
RD		+2.5V
OD		16.0V
RPhi :	Lo	-14V
	Hi	-4V
Dump Drain		+6V

The output FET Drain current was set to 2mA.

These potentials were recommended by EEV and are very close to the device maximums. The OD and Image Area clock lo potentials are very critical. The Dump Gate is treated as another vertical phase and is driven using the same potentials as for the Image Area clocks. When referring to EEV data sheets, note that all potentials are quoted relative to image area clock lo.

Appendix B : Dutch Controller Software Listing.

```
1  RAM-DISK 0

  0 ( DEFINE CLOCKS ) SEQUENCER DEFINITIONS DECIMAL ( smt 27 Jul 98)
  1 ( *** EEV42 CCD *** 2 CHIP MOSAIC *** O/P Left  CHANNEL A *** )
  2 9600 BAUD \ Baud rate for engineer's terminal
  3 00  0 CLOCK  TRACKA    ( TS0 )   01  1 CLOCK  ADC1      ( AC0 )
  4 02  0 CLOCK  SIG-SAMPA ( CS0 )   03  0 CLOCK  REF-SAMPA ( CR0 )
  5 04  1 CLOCK  SIG-RSTA  ( RS0 )   11  1 CLOCK  REF-RSTA  ( RR0 )
  6 17  1 CLOCK  CLAMPA    ( CL0 )   25  0 CLOCK  RSCKA     ( RSA )
  7 ( HA1)  23  1 CLOCK  1HCKA    \ Stored here as well - see VCLK
  8 ( HA2)  30  0 CLOCK  2HCKA    ( wrap board A - labelled H3 )
  9 ( HA3)  34  0 CLOCK  3HCKA    ( wrap board A - labelled H2 )
 10 ( HA4)  28  0 CLOCK  SWCKA
 11 ( VA1)  24  0 CLOCK  1VCKA    \ Store charge at V2
 12 ( VA2)  26  1 CLOCK  2VCKA    ( wrap board A - labelled V3 )
 13 ( VA3)  19  0 CLOCK  3VCKA    ( wrap board A - labelled V2 )
 14 ( VA4)  31  0 CLOCK  4VCKA
 15 ( VLA)  35  1 CLOCK  RD/IA  -->  \ V+ DF, V++ ND


2  RAM-DISK 0

  0 ( DEFINE CLOCKS ) SEQUENCER DEFINITIONS DECIMAL ( smt 20 Oct 98)
  1 ( *** EEV42 CCD *** 2 CHIP MOSAIC *** O/P Left  CHANNEL B *** )
  2
  3 07  0 CLOCK  TRACKB    ( TS1 )   08  1 CLOCK  ADC2      ( AC1 )
  4 05  0 CLOCK  SIG-SAMPB ( CS1 )   10  0 CLOCK  REF-SAMPB ( CR1 )
  5 13  1 CLOCK  SIG-RSTB  ( RS1 )   15  1 CLOCK  REF-RSTB  ( TR1 )
  6 12  1 CLOCK  CLAMPB    ( CL1 )   32  0 CLOCK  RSCKB     ( RSB )
  7 ( HB1)  21  1 CLOCK  1HCKB      \ Stored here as well - see V
  8 ( HB2)  27  0 CLOCK  2HCKB      ( wrap board A - labelled H3 )
  9 ( HB3)  14  0 CLOCK  3HCKB      ( wrap board A - labelled H2 )
 10 ( HB4)  16  0 CLOCK  SWCKB
 11 ( VB1)  22  0 CLOCK  1VCKB
 12 ( VB2)  36  1 CLOCK  2VCKB      ( wrap board A - labelled V3 )
 13 ( VB3)  20  0 CLOCK  3VCKB      ( wrap board A - labelled V2 )
 14 ( VB4)  29  0 CLOCK  4VCKB
 15 ( VLB)  33  1 CLOCK  RD/IB  -->  \ V+ DF, V++ ND


3  RAM-DISK 0

  0  ( Horizontal clock ) SEQUENCER                ( smt 20 Oct 98)
  1  0 SOR HCLOCK
  2             RSCKA 10 DF 20 ND
  3             1HCKA  5 DF 15 ND
  4             2HCKA 15 ND
  5             3HCKA 10 DF 15 ND
  6             SWCKA 10 DF 15 ND
  7             RSCKB 10 DF 20 ND
  8             1HCKB  5 DF 15 ND
  9             2HCKB 15 ND
 10             3HCKB 10 DF 15 ND
 11             SWCKB 10 DF 15 ND
 12  35 EOR
 13 HCLOCK >RAM
 14 \ Routine used for clearing and windowing.
 15 -->
```

```
ImageForth/68  V4.2.3a              CTRONIX/68008              26 Nov 98
_[H_[J

     4  RAM-DISK 0

       0 ( Idle routine     )          SEQUENCER         ( smt 12 Nov 98)
       1        1 SOR HRINT         \ Removes serial register spillage
       2
       3        RSCKA 25 ND        RSCKB 25 ND
       4        1HCKA  5 DF 15 ND  1HCKB  5 DF 15 ND
       5        2HCKA 15 ND        2HCKB 15 ND
       6        3HCKA 10 DF 15 ND  3HCKB 10 DF 15 ND
       7 \      4VCKA    1000  ND  4VCKB    1000  ND
       8
       9 1005 EOR HRINT >RAM
      10
      11
      12
      13
      14
      15                                      -->


     5  RAM-DISK 0

       0 ( Vertical clock ) SEQUENCER                   (  smt 12 Nov 98)
       1
       2 3 SOR  VCLOCK  \ RD/IA 100 ND
       3                \ RD/IB 100 ND
       4                1VCKA 300   DF 300   ND
       5                2VCKA 200   DF 300   ND
       6                3VCKA 100   DF 300   ND
       7
       8                1VCKB 300   DF 300   ND
       9                2VCKB 200   DF 300   ND
      10                3VCKB 100   DF 300   ND
      11
      12                3HCKA 950   ND 3HCKB 950 ND
      13 1002  EOR
      14 VCLOCK >RAM
      15 -->


     6  RAM-DISK 0

       0 ( Loading binned pixels                           smt 12 Oct 98)
       1 ( The next blocks hold the waveform changes for binned pixels )
       2 ( It require the X binning factor on the stack when loaded.)
       3
       4 ( This block holds parameters used to locate the required block)
       5
       6
       7 \ binning factors 2,3,4,8 only
       8
       9   BLK  @  1+ VHT BIN-BLOCK !
      10   4 SOR BIN
      11   3 FH LOAD
      12
      13 \ The BINNING routine only operates at the STANDARD readout
      14 \ speed, even if the CCDC has been set to another speed.
      15
```

```
ImageForth/68  V4.2.3a              CTRONIX/68008              26 Nov 98
_[H_[J

     7  RAM-DISK 0

       0 ( X BINNING TURBO SPEED 4+4  us CDS)  DECIMAL   ( smt 12 Oct 98)
       1 SEQUENCER VIA SEQUENCER FORTH ENDVIA DEFINITIONS
       2 : COMPILE-BIN-PIX ( xbin-factor - )    >R BIN SOR
       3   RSCKA      15 ND
       4   CLAMPA      5 DF  I 25 *  DF  5 DF 125 ND
       5   1HCKA       5 DF  I  0 DO  5 DF 15  ND  5 DF LOOP
       6   2HCKA       5 ND  I  0 DO 15 ND 10 DF       LOOP
       7   3HCKA       5 DF  I  0 DO  5 DF 15  ND  5 DF LOOP
       8   SWCKA       5 DF  I 25 * ND  55 ND 10 DF  65  ND
       9   REF-SAMPA   5 DF  I 25 * DF   5 DF 40 ND
      10   SIG-SAMPA   5 DF  I 25 * DF  80 DF 40 ND
      11   SIG-RSTA    5 DF  I 25 * DF   5 DF 125 ND
      12   REF-RSTA    5 DF  I 25 * DF   5 DF 125 ND
      13   TRACKA      5 DF  I 25 * DF  80 DF  45 ND
      14   ADC1        5 DF  I 25 * DF 125 DF 5 ND
      15 [                                                    -->


     8  RAM-DISK 0

       0 ( X BINNING TURBO SPEED  4+4 us CDS)  DECIMAL   ( smt 12 Oct 98)
       1  ]  ( needed since routine requires 2 ram-disk blocks )
       2   RSCKB      15 ND
       3   CLAMPB      5 DF  I 25 * DF   5 DF 125 ND
       4   1HCKB       5 DF  I  0 DO  5 DF 15  ND  5 DF LOOP
       5   2HCKB       5 ND  I  0 DO 15 ND 10  DF       LOOP
       6   3HCKB       5 DF  I  0 DO  5 DF 15  ND  5 DF LOOP
       7   SWCKB       5 DF  I 25 * ND   55 ND  10 DF   65 ND
       8   REF-SAMPB   5 DF  I 25 * DF   5 DF 40  ND
       9   SIG-SAMPB   5 DF  I 25 * DF  80 DF 40  ND
      10   SIG-RSTB    5 DF  I 25 * DF   5 DF 125 ND
      11   REF-RSTB    5 DF  I 25 * DF   5 DF 125 ND
      12   TRACKB      5 DF  I 25 * DF  80 DF  45 ND
      13   ADC2        5 DF  I 25 * DF 125 DF   5 ND
      14              R> 25 * 135 +         EOR BIN >RAM ;
      15 COMPILE-BIN-PIX BIN-TEMP FORGET COMPILE-BIN-PIX


     9  RAM-DISK 0

       0 ( STANDARD SPEED 8+8 us CDS )    CR  SEQUENCER (  smt 06 Nov 98)
       1 12 SOR SP0
       2 RSCKA      13 ND                  RSCKB     13 ND
       3 CLAMPA     25 DF 220 ND           CLAMPB    25 DF 220 ND
       4 1HCKA       5 DF  15 ND           1HCKB      5 DF  15 ND
       5 2HCKA      15 ND                  2HCKB     15 ND
       6 3HCKA       5 DF  15 ND           3HCKB      5 DF  15 ND
       7 SWCKA       5 DF 125 ND  10 DF 105 ND
       8 SWCKB       5 DF 125 ND  10 DF 105 ND
       9 REF-SAMPA  35 DF  80 ND          REF-SAMPB   35 DF  80 ND
      10 SIG-SAMPA 150 DF  80 ND          SIG-SAMPB  150 DF  80 ND
      11 SIG-RSTA   25 DF 220 ND          SIG-RSTB    25 DF 220 ND
      12 REF-RSTA   25 DF 220 ND          REF-RSTB    25 DF 220 ND
      13 TRACKA    150 DF  85 ND          TRACKB     150 DF  85 ND
      14 ADC1 240 DF  5 ND                ADC2 240 DF  5 ND
      15 246 EOR         SP0 >RAM       -->
```

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ImageForth/68  V4.2.3a              CTRONIX/68008              26 Nov 98
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    10  RAM-DISK 0

       0  ( QUICK speed 6 + 6us CDS )        SEQUENCER   ( smt 22 Oct 98)
       1 7 SOR SP1
       2 RSCKA      13 ND                  RSCKB     13 ND
       3 CLAMPA     25 DF 180 ND           CLAMPB    25 DF 180 ND
       4 1HCKA       5 DF  15 ND           1HCKB      5 DF  15 ND
       5 2HCKA      15 ND                  2HCKB     15 ND
       6 3HCKA       5 DF  15 ND           3HCKB      5 DF  15 ND
       7 SWCKA       5 DF  95 ND  10 DF  95 ND
       8 SWCKB       5 DF  95 ND  10 DF  95 ND
       9 REF-SAMPA  35 DF  60 ND         REF-SAMPB   35 DF  60 ND
      10 SIG-SAMPA 125 DF  60 ND         SIG-SAMPB  125 DF  60 ND
      11 SIG-RSTA   25 DF 180 ND         SIG-RSTB    25 DF 180 ND
      12 REF-RSTA   25 DF 180 ND         REF-RSTB    25 DF 180 ND
      13 TRACKA    125 DF  65 ND         TRACKB  125 DF 65 ND
      14 ADC1 200 DF  5 ND              ADC2 200 DF  5 ND
      15 206 EOR         SP1 >RAM         -->


    11  RAM-DISK 0

       0  ( TURBO SPEED 4 + 4 us CDS )         SEQUENCER ( smt 06 Nov 98)
       1 8 SOR SP2
       2 RSCKA      13 ND                  RSCKB     13 ND
       3 CLAMPA     23 DF 135 ND           CLAMPB    23 DF 135 ND
       4 1HCKA       5 DF  15 ND           1HCKB      5 DF  15 ND
       5 2HCKA      15 ND                  2HCKB     15 ND
       6 3HCKA       5 DF  15 ND           3HCKB      5 DF  15 ND
       7 SWCKA       5 DF  68 ND  10 DF  75 ND
       8 SWCKB       5 DF  68 ND  10 DF  75 ND
       9 REF-SAMPA  30 DF  40 ND         REF-SAMPB  30  DF  40 ND
      10 SIG-SAMPA  98 DF  40 ND         SIG-SAMPB  98  DF  40 ND
      11 SIG-RSTA   23 DF 135 ND         SIG-RSTB   23  DF 135 ND
      12 REF-RSTA   23 DF 135 ND         REF-RSTB   23  DF 135 ND
      13 TRACKA     98 DF  45 ND         TRACKB  98 DF 45 ND
      14 ADC1 153 DF  5 ND              ADC2 153 DF  5 ND
      15 159 EOR            SP2 >RAM     -->


    12  RAM-DISK 0

       0 ( NONASTRO SPEED 3 + 3 us ) SEQUENCER  (          smt 06 Nov 98)
       1   2 SOR SP3
       2   RSCKA       13 ND                   RSCKB      13 ND
       3   1HCKA        5 DF        15 ND      1HCKB       5 DF   15 ND
       4   2HCKA       15 ND                   2HCKB      15 ND
       5   3HCKA        5 DF        15 ND      3HCKB       5 DF   15 ND
       6   REF-SAMPA   25 DF        30 ND      REF-SAMPB  25 DF   30 ND
       7   SIG-SAMPA   83 DF        30 ND      SIG-SAMPB  83 DF   30 ND
       8   SWCKA        5 DF 60 ND 8 DF 53 ND
       9   SWCKB        5 DF 60 ND 8 DF 53 ND
      10   TRACKA      83 DF        35 ND      TRACKB     83 DF   35 ND
      11   ADC1       123 DF         4 ND      ADC2      123 DF    4 ND
      12   CLAMPA      25 DF       100 ND      CLAMPB     25 DF  100 ND
      13   SIG-RSTA    25 DF       100 ND      SIG-RSTB   25 DF  100 ND
      14   REF-RSTA    25 DF       100 ND      REF-RSTB   25 DF  100 ND
      15   138 EOR SP3 >RAM   -->
```

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    13  RAM-DISK 0

       0 ( FLASH     Clear of CCD )            SEQUENCER ( smt 12 Nov 98)
       1  9 SOR FLASH-CLR
       2     \       RD/IA  350 ND          RD/IB   350 ND
       3             1VCKA  150 DF  150 ND  1VCKB   150 DF  150 ND
       4             2VCKA  100 DF  150 ND  2VCKB   100 DF  150 ND
       5             3VCKA   50 DF  150 ND  3VCKB    50 DF  150 ND
       6       \     4VCKA  400 ND          4VCKB   400 ND
       7             RSCKA  400 ND          RSCKB   400 ND
       8             1HCKA  400 DF          1HCKB   400 DF
       9             2HCKA  400 ND          2HCKB   400 ND
      10             3HCKA  400 ND          3HCKB   400 ND
      11             SWCKA  400 ND          SWCKB   400 ND
      12   402 EOR FLASH-CLR >RAM
      13
      14
      15 -->


    14  RAM-DISK 0

       0  ( DUMMY PIXEL ROUTINE 1+1us CDS)     SEQUENCER ( smt 06 Nov 98)
       1 10 SOR DUMMY-PIXEL
       2 RSCKA      13 ND                RSCKB     13 ND
       3 CLAMPA     15 DF  59 ND         CLAMPB    15 DF  59 ND
       4 1HCKA       4 DF  10 ND         1HCKB      4 DF  10 ND
       5 2HCKA       9 ND                2HCKB      9 ND
       6 3HCKA       4 DF  10 ND         3HCKB      4 DF  10 ND
       7 SWCKA       5 DF  26 ND   8 DF  35 ND
       8 SWCKB       5 DF  26 ND   8 DF  35 ND
       9 REF-SAMPA  18 DF  10 ND       REF-SAMPB   18 DF  10 ND
      10 SIG-SAMPA  44 DF  10 ND       SIG-SAMPB   44 DF  10 ND
      11 SIG-RSTA   15 DF  59 ND       SIG-RSTB    15 DF  59 ND
      12 REF-RSTA   15 DF  59 ND       REF-RSTB    15 DF  59 ND
      13
      14
      15 185 EOR DUMMY-PIXEL >RAM        -->


    15  RAM-DISK 0

       0 ( Very Fast Clear of CCD-NOT USED)    SEQUENCER ( smt 12 Nov 98)
       1     11 SOR QUICK-CLR
       2
       3             1VCKA  150 DF  150 ND  1VCKB   150 DF  150 ND
       4             2VCKA  100 DF  150 ND  2VCKB   100 DF  150 ND
       5             3VCKA   50 DF  150 ND  3VCKB    50 DF  150 ND
       6             4VCKA  400 ND          4VCKB   400 ND
       7             RSCKA  400 ND          RSCKB   400 ND
       8             1HCKA  400 DF          1HCKB   400 DF
       9             2HCKA  400 ND          2HCKB   400 ND
      10             3HCKA  400 ND          3HCKB   400 ND
      11             SWCKA  400 ND          SWCKB   400 ND
      12   402 EOR QUICK-CLR >RAM
      13 \ Actually does a V clock triplet and at the same time sets the
      14 \ serial register all high. RUN 2 X NO. OF ROWS
      15 -->
```

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    16  RAM-DISK 0

       0 \ ( IDLE+IMO   routine    )  SEQUENCER         (      06 Nov 93)
       1 \ --> 12 SOR ABM-CLK
       2 \      RD/IA  32000 ND          RD/IB 32000 ND
       3 \      RSCKA  32000 ND   SWCKA  32000 ND
       4 \      1HCKA  32000 ND   1HCKB  32000 ND
       5 \      2HCKA  32000 DF   2HCKB  32000 DF
       6 \      3HCKA  32000 ND   3HCKB  32000 ND
       7 \      RSCKB  32000 ND   SWCKB  32000 ND
       8 \      1VCKA   4000 DF  8000 ND   1VCKB   4000 DF  8000 ND
       9 \      2VCKA   6000 DF  4000 ND   2VCKB   6000 DF  4000 ND
      10 \      3VCKA  32000 DF   3VCKB  32000 DF
      11 \      4VCKA  32000 ND   4VCKB  32000 DF
      12 \ 30002 EOR ABM-CLK >RAM   -->    \ MAX LENGTH
      13 \ ROUTINE PREVENTS COLUMN BLOOMING FROM SATURATED STAR.
      14 \ V++ SWITCHED TO V+ WHICH IS OPTIMISED FOR EACH CCD
      15 -->


    17  RAM-DISK 0

       0  ( SETUP FUNCTIONS.                                 smt 12 Nov 98)
       1 SP0                SET-SPEED0  \ Standard speed function
       2 SP1                SET-SPEED1  \ Quick speed
       3 SP2                SET-SPEED2  \ turbo
       4 SP3                SET-SPEED3  \ nonastro
       5 SP0                SET-SPEED4  \ NOT USED WAS CCD1 ONLY
       6 BIN                SET-BIN     \ Binning function
       7 DUMMY-PIXEL        SET-DPIX    \ Dummy pixel routine
       8 HCLOCK             SET-HCLK    \ H clock
       9 VCLOCK             SET-VCLK    \ V clock
      10 HRINT              SET-HIDLE   \ IDLE ONLY
      11
      12
      13
      14 QUICK-CLR         SET-QCLR
      15 FLASH-CLR         SET-FCLR --> \ FLASH CLEAR


    18  RAM-DISK 0

       0  ( Customisations for 2 CHIP CAMERA )  (          smt 06 Nov 98)
       1 1P  2 1 I-OFFSET ! 99 1 OD-ZERO !        \ IS,OD Offset = Ch. 1
       2 1P  3 2 I-OFFSET ! 99 2 OD-ZERO !        \ Ch. 2
       3
       4
       5 1P 2016 'ZERO-AD !  30 'SERVO-ZERO !     \ 1unit=-0.16degC
       6 C1(ABG) SEQ-BREG CLR-BIT                 \ 2 CH. FOR ABG TGUP
       7 98 YEAR W! NETWORK CCD1  40 PREFLASH-SCALER !
       8 ( ********************************************************* )
       9 1V 2148 4128 13 NEW-TYPE EEV48        EEV48         \ CCD TYPE
      10 ( *********** DO NOT EDIT LINE 9  OF THIS BLOCK ************** )
      11 : HOPG 2 OPG ; : LOPG 1 OPG ;
      12
      13 50 QUICK-VCLKS/LINE !  \ 40  '#CLR-VCLK ! \ New CLEAR algorithm
      14 FORTH DEFINITIONS PAGE ." TWO CHIP MOSAIC CAMERA     "  500 MS
      15 : ENBT 1 'SILENT W! VT100  RAM-DISK 1  LIST ; I'M smt    -->
```

```
Chip 0 Configuration.

Virtual head number 1

Serial number is :- EEV 7461-14-6 (CCD 1)

0         0.00 Volts  Channel   0
 1        0.00 Volts  Channel   0
 2        0.00 Volts  Channel   0
 3        0.00 Volts  Channel   0
 4        0.00 Volts  Channel   0
 5        0.00 Volts  Channel   0
 6        0.00 Volts  Channel   0
7         0.00 Volts  Channel   0
V+S0    -17.70 Volts  Channel   8
V-0     -16.00 Volts  Channel   9
V+0      -4.00 Volts  Channel  10
V-SL      2.40 Volts  Channel  11
RD0       2.50 Volts  Channel  12
VSS0     -6.00 Volts  Channel  13
OG      -14.00 Volts  Channel  14
V++0     -4.00 Volts  Channel  15
R-S0      2.00 Volts  Channel  16
R-0     -13.00 Volts  Channel  17
R+0      -4.00 Volts  Channel  18
R+S0    -18.00 Volts  Channel  19
ODL0      7.00 Volts  Channel  20
ODH0     16.20 Volts  Channel  21
OGH     -13.00 Volts  Channel  22
OGL       3.00 Volts  Channel  23
N/C1      0.00 Volts  Channel  24
BG        7.00 Volts  Channel  25
DUMP      6.00 Volts  Channel  26
H++0     -4.00 Volts  Channel  27
H+0      -4.00 Volts  Channel  28
H-      -14.50 Volts  Channel  29
H-S0      2.00 Volts  Channel  30
H+S0    -18.00 Volts  Channel  31
<CCD1> ok

>
```

```
Chip 1 Configuration.

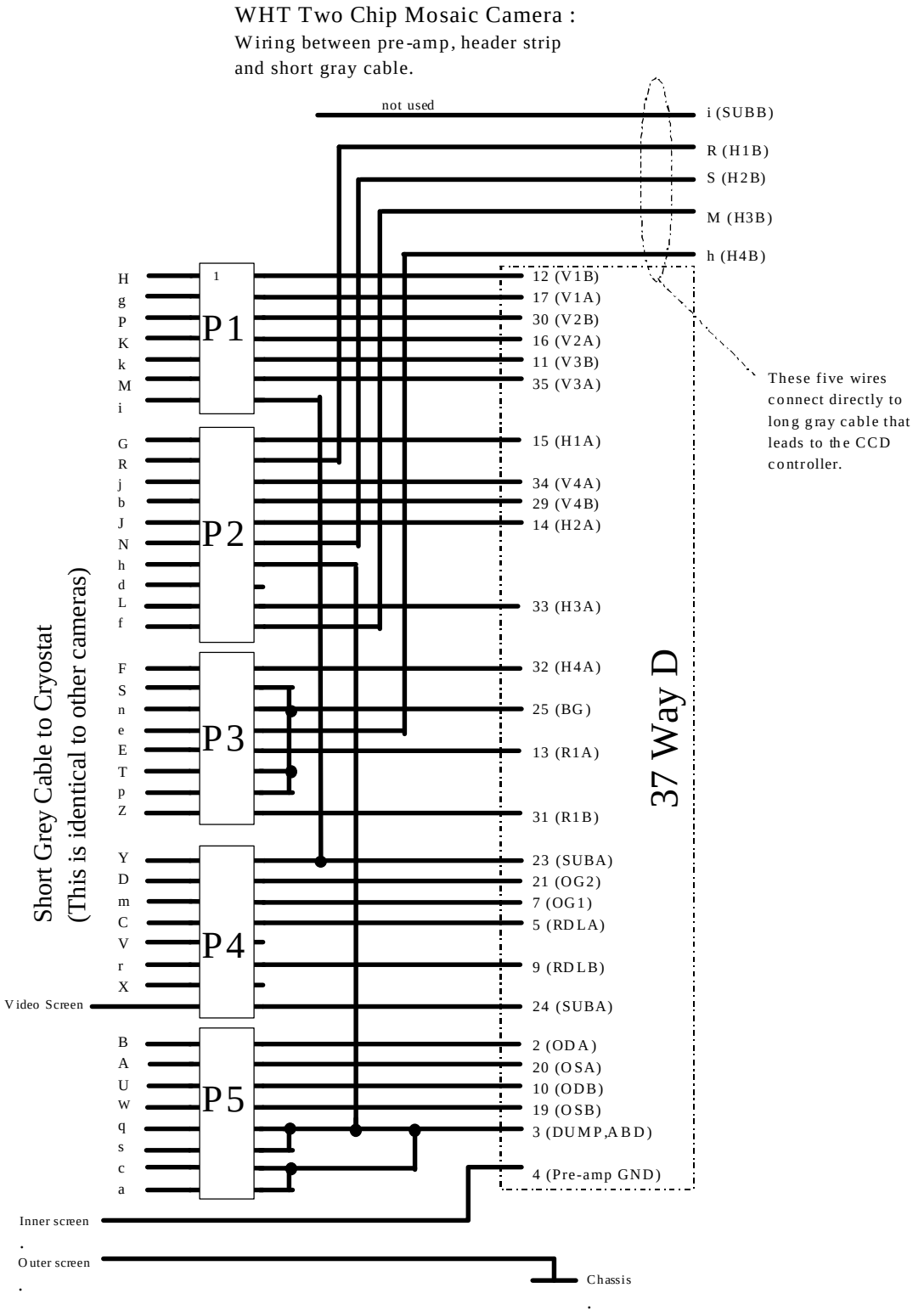
Virtual head number 1

Serial number is :- EEV 7461-11-6 (CCD 2)

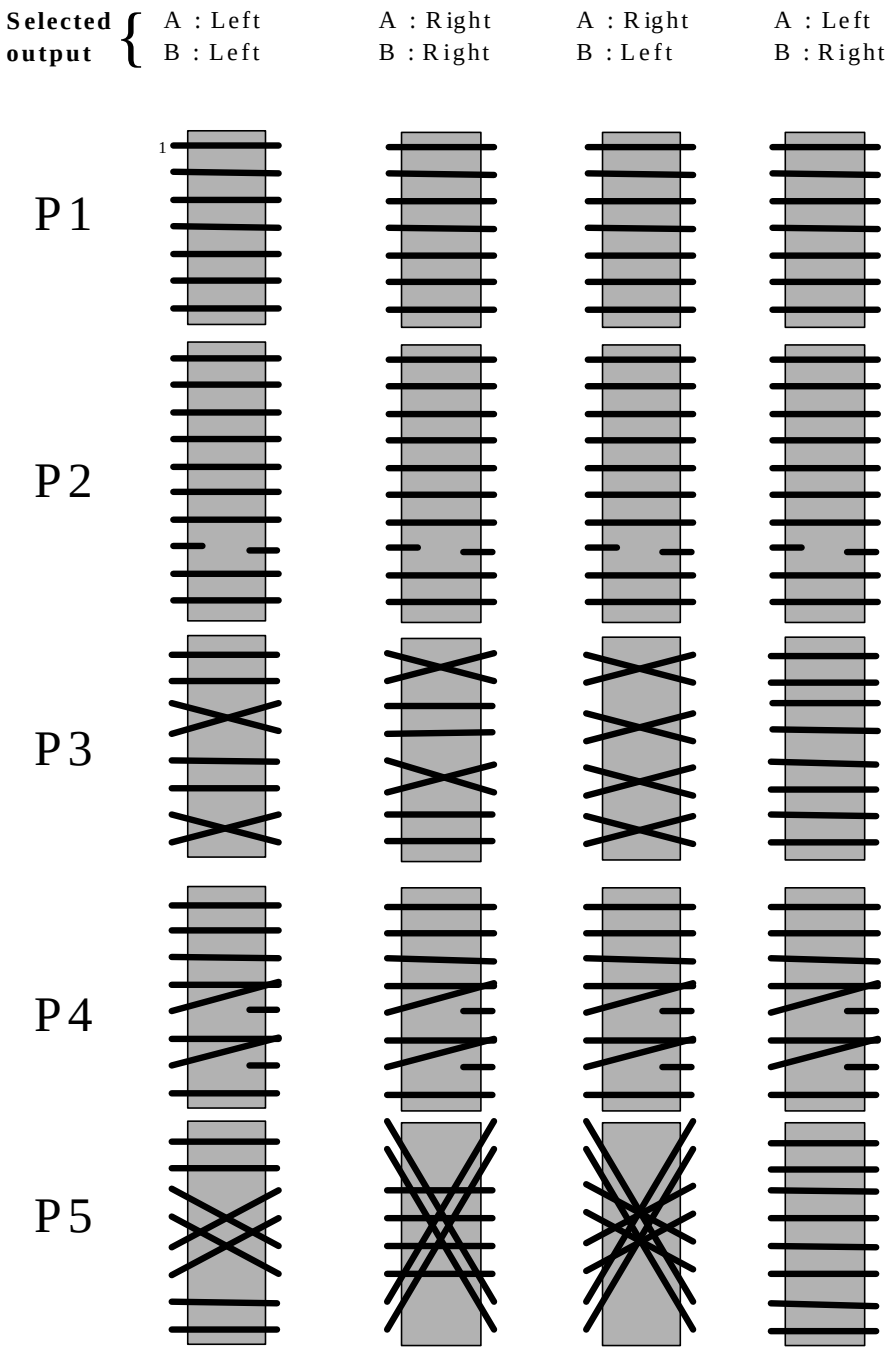
0        0.00 Volts  Channel   0
 1       0.00 Volts  Channel   0
 2       0.00 Volts  Channel   0
 3       0.00 Volts  Channel   0
 4       0.00 Volts  Channel   0
 5       0.00 Volts  Channel   0
 6       0.00 Volts  Channel   0
 7       0.00 Volts  Channel   0
V+S1   -17.70 Volts  Channel  40
V-1    -16.00 Volts  Channel  41
V+1     -4.00 Volts  Channel  42
V-S1     2.40 Volts  Channel  43
RD1      2.25 Volts  Channel  44
VSS1    -6.00 Volts  Channel  56
N/C2     0.00 Volts  Channel  46
V++1    -4.00 Volts  Channel  47
R-S1     2.00 Volts  Channel  48
R-1    -13.00 Volts  Channel  49
R+1     -4.00 Volts  Channel  50
R+S1   -18.00 Volts  Channel  51
ODL1     7.00 Volts  Channel  52
ODH1    16.30 Volts  Channel  53
N/C3     0.00 Volts  Channel  54
N/C6     0.00 Volts  Channel  55
N/C4     0.00 Volts  Channel  45
N/C7     0.00 Volts  Channel  57
N/C5     0.00 Volts  Channel  58
H++1    -4.00 Volts  Channel  59
H+1     -4.00 Volts  Channel  60
H-1    -14.50 Volts  Channel  61
H-S1     2.00 Volts  Channel  62
H+S1   -18.00 Volts  Channel  63
<CCD1> ok

>
```

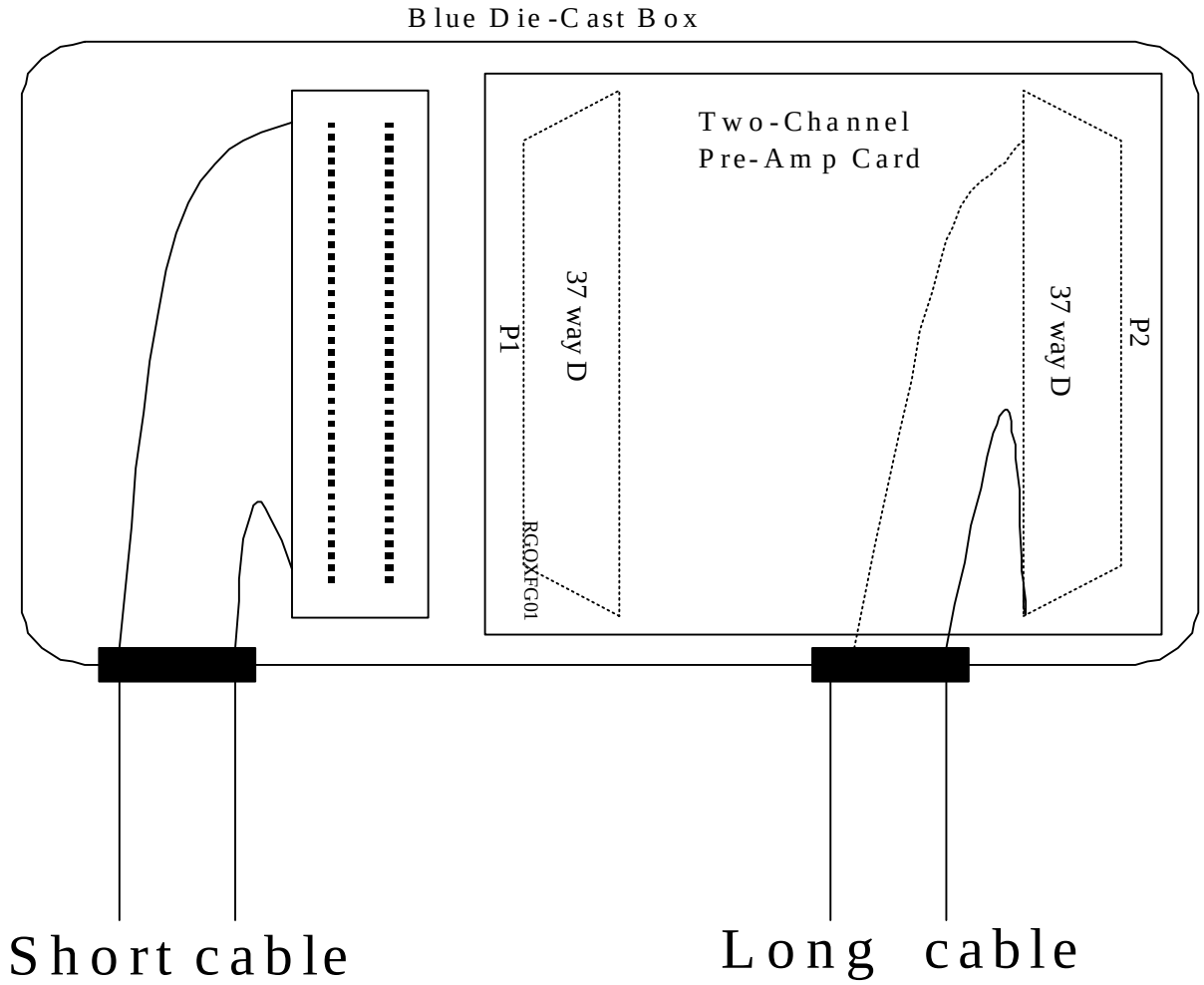
Appendix C. Wiring Details for Dutch controller



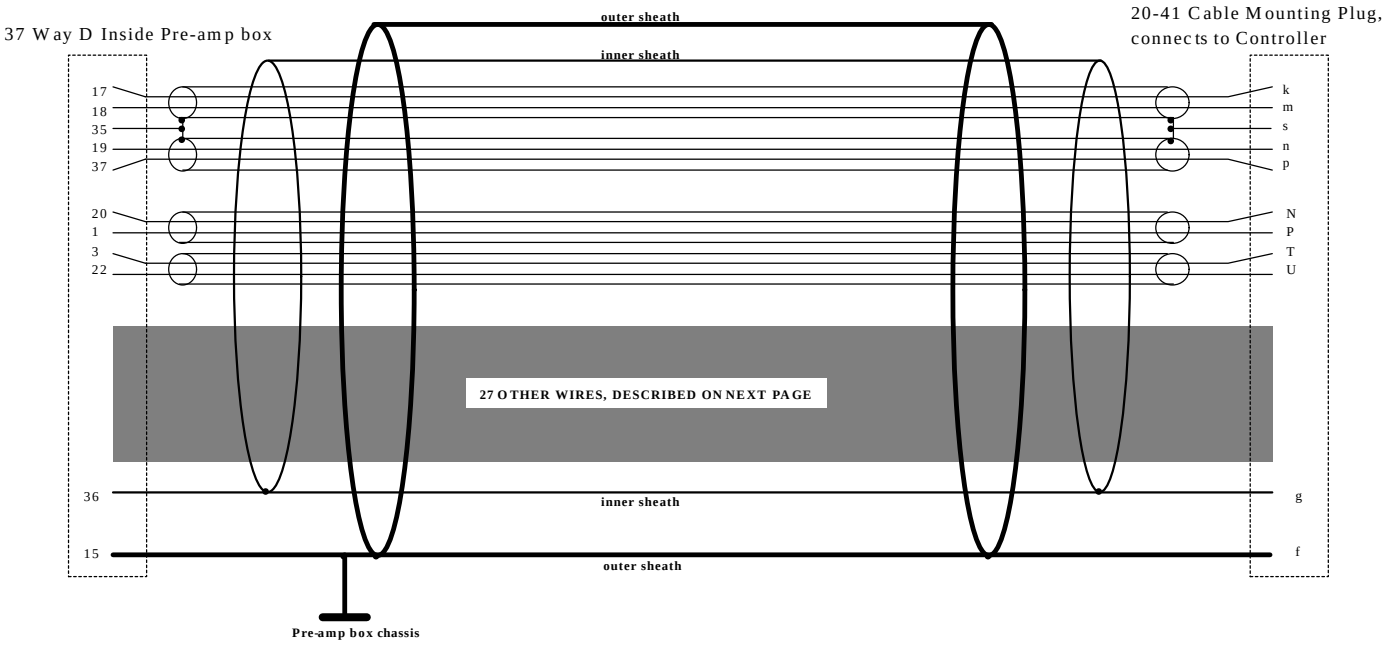
WHT Two Chip Mosaic Camera :
Pre-amp header link configurations



WHT Two Chip Mosaic Camera:
Orientation of Pre-Amp PCB

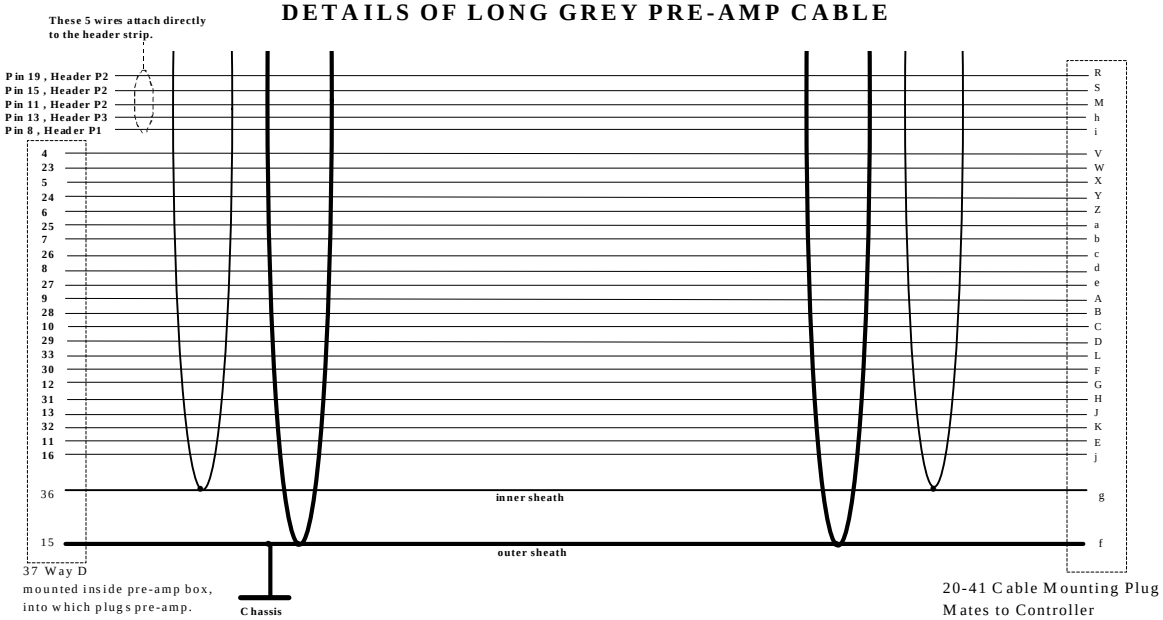


DETAILS OF LONG GREY PRE-AMP CABLE



WHT MOSAIC CAMERA PRE-AMP CABLING SIMON TULLOCH ATC SEP 98

DETAILS OF LONG GREY PRE-AMP CABLE



WHT MOSAIC CAMERA PRE-AMP CABLING SIMON TULLOCH ATC SEP 98

WHT Two Chip Mosaic Camera:

Wiring internal to cryostat

		'X'	'Y'	'X'	Y'
	cryo	chip 1	chip 2	chip 1	chip 2
CCD Sig	20-41	21 way	21 way	15 way	15 way
P1B	H		15		
P1A	g	15			
P2B	P		14		
P2A	K	14			
P3B	k		16		
P3A	M	16			
H1A	G	5,8			
H1B	R		5,8		
DGA(V4A)	j	2,10			
DGB(V4B)	b		2,10		
H2A	J	4,7			
H2B	N		4,7		
DUMP(ABD)	h			1,8	1,8
H3A	L	6			
H3B	f		6		
SWLA	F	1			
SWRA	S	11			
SWLB	n		1		
SWRB	e		11		
RLA	E	3			
RRA	T	9			
RLB	p		3		
RRB	Z		9		
SUBA	Y	13		13	
OG2	D			3,6	3,6
OG1	m	12,21	12,21		
RDLA	C			2	
RDRA	V			7	
RDLB	r				2
RDRB	X				7
ODLA	B			9	
OSLA	A			10	
ODRB	U				15
OSRB	W				14
ODLB	q				9
OSLB	s				10
ODRA	c			15	
OSRA	a			14	
SUBB	i	<- after thought	13		13
N/C		17,18,19,20	17,18,19,20	4,5,11,12	4,5,11,12

2 spare pins in the 20-41

WHT Two Chip Mosaic Camera:
Front Panel CCD Controller Wiring

	Connector from CCDC cards to front panel 20-41								
		clock	clock	CDS	CDS		Channel	Channel	
	20-41	Function	board 0	board 1	board 0	board 1		SEQ A	SEQ B	DAC Channel
	A	V3b		26					20	
	B	V4b		28					29	
	C	RDb		22						44
spare ->	D	(RDRa)	10							
	L	ODa	14							20 odint, 21 odrd
	F	BG	7							25
	G	RDa	22							12
	H	SUBa	23							13
	J	ABD(DMP)	8							26
	i	SUBb		10						56
	E	OG1	21							14
	M	H3b		3					14	
	N	minus 9V			1,2					
	P	plus 9V			5,6					
	R	H1b		2					21	
	S	H2b		4					27	
	T	V1a	25					24		
	U	V3a	26					19		
	V	V2a	27					26		
	W	V4a	28					31		
	X	H1a	2					23		
	Y	H3a	3					34		
	Z	H2a	4					30		
	a	H4a	5					28		
	b	R1a	18					25		
	c	R1b		18					32	
	d	V1b		25					22	
	e	V2b		27					36	
	f	chassis								
	g	clk gnd	6,11,19,24							
	h	H4b		5					16	
	K	OG2	12							22 odint, 23 odrd
	k	pre-out +			8					
	m	pre-out -			7					
	n	pre-out -				7				
	p	pre-out +				8				
	q	spare								
	r	spare								
	s	video screen			3,4,9					
	t	spare								
	j	ODb		14						52 odint, 53 odrd

Thiswas fixed from the APO design by the following changes :
1) line i presently goes to 37 way D pin 16 in pre-amp, reconnect to pin 10 on p4 on header strip
2) line K connect to pin 32 on 37 way pre-amp D
3) line j currently goes to pin 32 on 37way pre-amp D, reconnect to pin 16

NB H3 and H2, V2 and V3 on wire wrap pins near backplane connector of clock boards have transposed labels.

WHT Two Chip Mosaic Camera:

Dutch Controller Clock Board Wiring

The following tables show the connections needed between the two rows of wire-wrap pins at the end of the clock boards

Board 0 (CCD 1)

Left Pin	Right Pin	Function	SEQUENCER CHANNEL
H1	25D	1HCKA	23
H2	30C	2HCKA	30
H3	29D	3HCKA	34
H4	30B	SWCKA	28
V1	27C	1VCKA	24
V2	27A	2VCKA	19
V3	27B	3VCKA	26
V4	28C	4VCKA	31
V+	32A	RD/IA	35
H+	24A		18
C0	19B	ODRD/ODINT	
C1	28B	LOPG/HOPG	
R1	30A	R1A	25
R2	dont care		

This is the same as a normal clock board
i.e. this board could be replaced with a clock board from any other EEV CCD controller.

Board 1 (CCD 2)

Left Pin	Right Pin	Function	SEQUENCER CHANNEL
H1	24C	1HCKB	21
H2	22A	2HCKB	27
H3	31A	3HCKB	14
H4	25A	SWCKB	16
V1	25B	1VCKB	22
V2	26C	2VCKB	36
V3	32B	3VCKB	20
V4	27D	4VCKB	29
V+	32C	RD/IB	33
H+	dont care		
C0	19B	ODRD/ODINT	
C1	dont care		
R1	31	R1B	32
R2	dont care		

This is heavily modified.

Cryostat Temperature Connector

Amphenol 12-10 connector

A Heater +
B Heater -
C LED +
D LED -
E Temp Sense ground
F Temp sense
G Temp sense ref.
H Temp sense +10V

The heater is a 100 Ohm power resistor. The temperature sensor is built into a bridge arrangement inside the cryostat. Its resistance can be measured directly between pins E and F. It is a Pt100 sensor with a coefficient of -0.4046 Ohms per degree C. The internal LEDS have no current limiting resistors, a current of 5mA for about 1s will give a deep exposure.