RGO Technical Note 117
CCD Camera EEV #12

Simon Tulloch. 17 June 1998

CONTENTS

1. General Description.

CCD Device Number A5500-5
CCD Device Type EEV4280. Thinned and AR Coated.
13.5µm pixels. 2148 x 4128 Pixels total. 50 x-underscan, 50 x-overscan, 28 y-overscan.
Two working amplifiers, 4 and 5 electrons RMS noise.
Cosmetically clean with 1 bright column only.
QE=65% at 380nm, 81% at 400nm, 80% at 650nm, 14% at 950nm.
Dark current= 0.75e/hour at -120C.
Full Well= 240,000 electrons

2. Operational Modes.

The EEV42-80 devices have an on-chip gain switch that can reduce output node sensitivity by a factor of approximately 2.8. The default state is hi-sensitivity mode which minimises readout noise and gives an output sensitivity of about 4.5µV / electron. This mode is recommended for spectroscopic applications. Lo-sensitivity mode can be selected at the CCD engineering terminal (see below) and allows the full dynamic range of the CCD to be utilised. In this mode, which is recommended for prime focus imaging, the CCD full-well signal matches closely the input range of the ADC. Readout noise rises to approximately 10e RMS but in most direct imaging applications this will be insignificant next to sky noise.

To select Hi-Gain Mode (default) type : **'hopg'**
To select Lo-Gain Mode (default) type : **'lopg'**
To read back Mode setting type : **'see'**

An Anti-Blooming (AB) operational mode is also implemented for this camera although the default state has it switched off. When enabled (see below) the vertical clock phases 1 and 2 are modulated so that the integrated charge in each pixel is 'wobbled' back and forth. Excess charge that would otherwise produce a bloomed feature is removed by this process, which is thought to involve the injection of holes from the CCD channel stops. Each 'wobble' cycle can remove >200 electrons. The wobble frequency used for this device was 330 Hz. The drawback of AB clocks is that a large number (>4500) of bright spot features are generated in the image. One very bright saturated LED type defect is also created close to the left hand amplifier. Due to these drawbacks, the use of AB mode is not really recommended for scientific imaging.

To switch AB clocks on type at the engineering terminal : **1 VHT 'ANTI-BLOOM C!**

To switch off **: 0 VHT 'ANTI-BLOOM C!**

To check present setting **: VHT 'ANTI-BLOOM C?**

3. Image Quality.

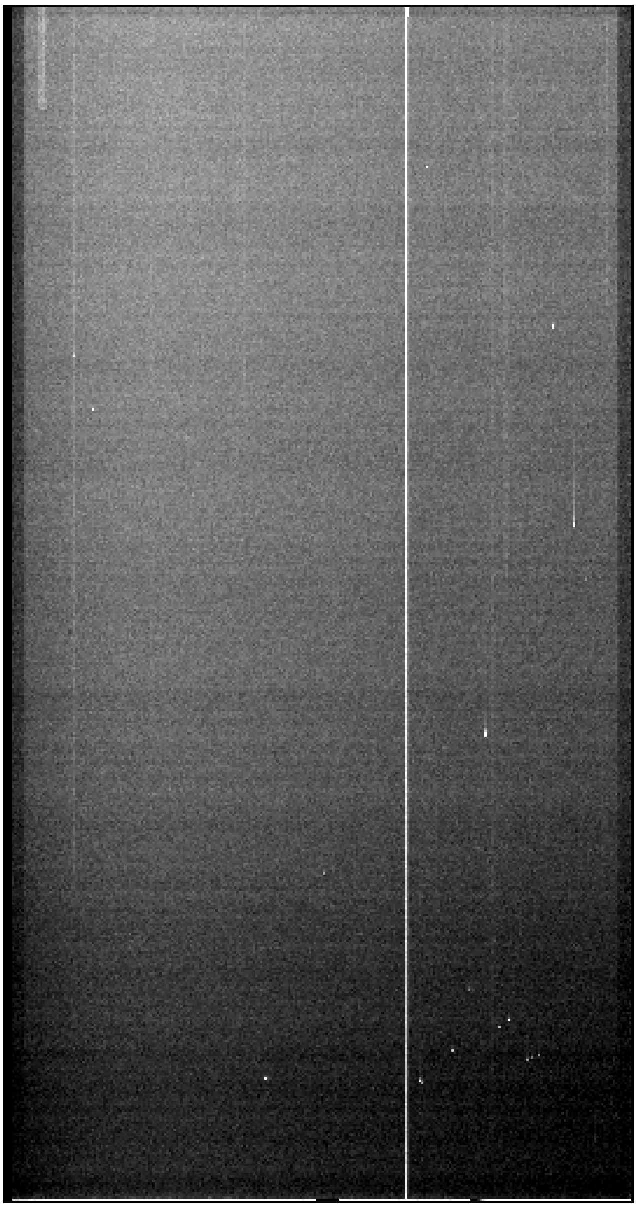
Image quality was assessed from a series of five 600s dark frames. These were combined into one image using the IRAF 'imcombine' function with parameter 'reject' set equal to 'minmax' in order to reject cosmic ray features. Bright columns were then located by manual inspection of the resultant image. The IRAF functions 'daofind' and 'daophot' were then used to log isolated 'hot' pixels. The locations of the defects recorded in this section have co-ordinates referenced to the left hand CCD amplifier.

Measurement temperature was -120C.

3.1. Defective Columns.

A bright feature near the top right of the image spills charge down column 1376. A trap cluster just visible on the top left of the image blocks all signal that is vertically transferred through it.

600 second dark frame



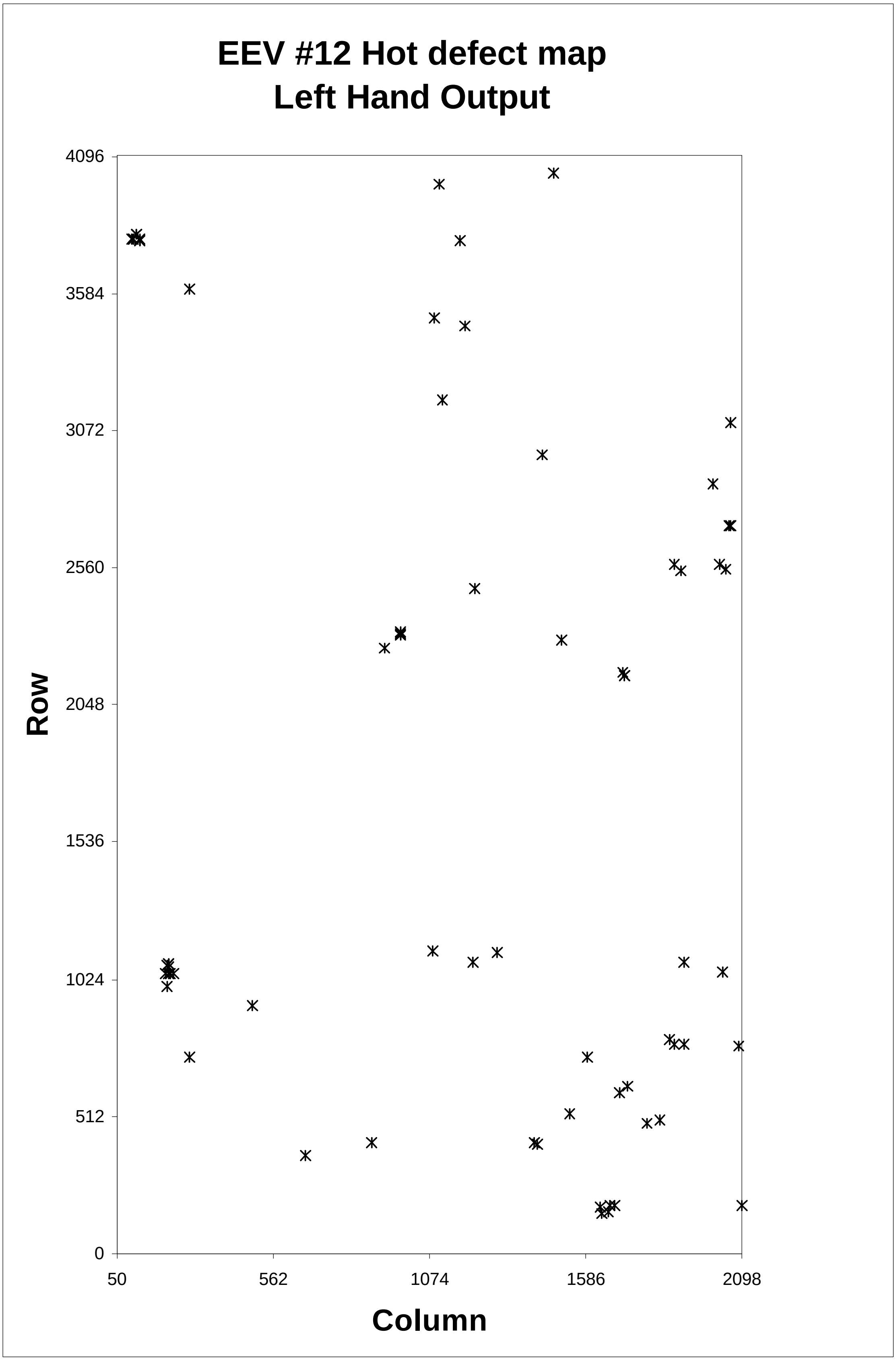
3.2. Hot Spots.

The size and location , referenced to the left hand CCD amplifier, of significant hot spots is tabulated below and shown graphically on the following page.

X-Coord	Y-Coord	electrons after 600s	electrons after 300s
1640	150	612	345
1660	158	232	133
1633	172	122	56
2098	178	195	128
1665	180	4605	2296
1679	180	376	128
668	366	288	182
1428	407	248	186
1418	416	455	67
884	417	179	460
1788	486	142	238
1827	501	217	142
1535	522	169	237
1695	602	205	210
1723	628	332	374
286	735	74	0
1591	736	186	234
2089	778	103	43
1878	779	145	102
1907	779	1110	465
1860	798	211	116
495	926	931	434
211	999	1022	445
211	1043	162	62
219	1047	180	92
226	1047	628	334
233	1047	450	252
2035	1052	292	197
219	1073	4672	2283
214	1077	141	111
217	1084	2221	1112
220	1083	4474	2240
1216	1088	319	118
1910	1091	184	112
1296	1126	185	160
1087	1131	200	205
1710	2161	245	173
1715	2161	1525	809
1707	2172	2802	1423
927	2262	691	349
1507	2292	261	286
979	2310	943	465
979	2317	465	174

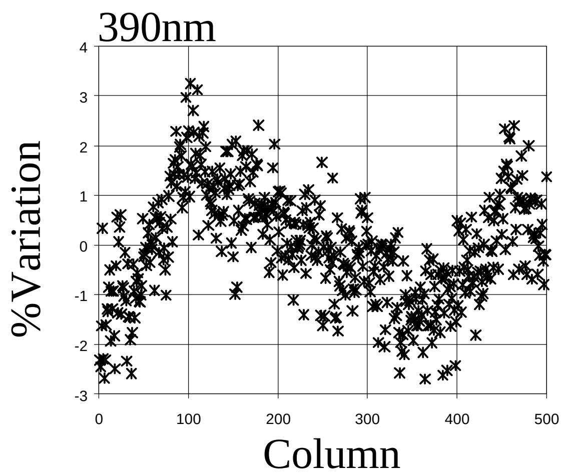
X-Coord	Y-Coord	electrons after 600s	electrons after 300s
979	2321	84	41
1222	2481	171	86
1897	2548	125	130
2043	2553	80	25
1876	2570	150	103
2023	2570	90	20
2057	2715	667	342
2060	2715	512	234
2003	2872	207	129
1441	2979	806	417
2062	3100	23273	11521
1116	3186	22	38
1190	3465	409	182
1088	3495	60	48
290	3604	368	171
122	3779	23726	11871
123	3779	21432	10739
1177	3782	97	49
102	3785	3097	1482
100	3788	9204	4660
104	3788	4838	2291
123	3788	1672	835
113	3804	2506	1156
116	3804	2654	1224
1107	3992	919	427
1482	4031	3607	1718
1376	3811	>240000	>240000

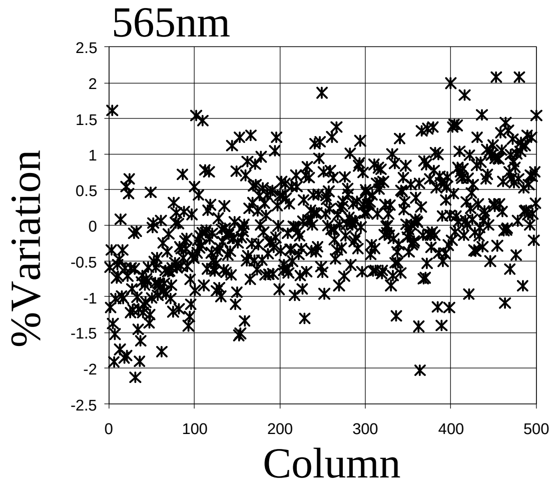
In addition to these hot spots , a sea level cosmic ray flux of 1940 events per hour was measured (2.2 events cm^{-2} min^{-1}).

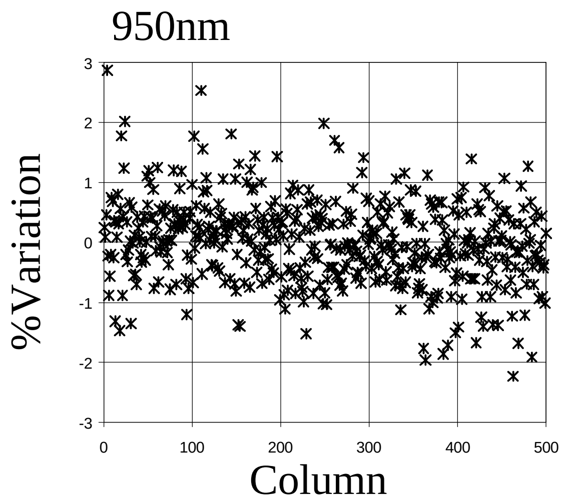

EEV #12 Hot defect map
Left Hand Output
Row
Column
4096
3584
3072
2560
2048
1536
1024
512
0
50
562
1074
1586
2098

3.3. Pixel Response Non-Uniformity (PRNU).

This was measured at three wavelengths using the RGO flat field projector. The exposures were sufficiently deep to reduce photon noise below 0.2% , thus revealing the intrinsic pixel-pixel sensitivity variations. A cross-hatch pattern was visible in the 390nm exposures, thought to be due to laser annealing. The sensitivity variation here was +/- 2%. At longer wavelengths this patterning disappeared and the PRNU dropped to +/- 1%.



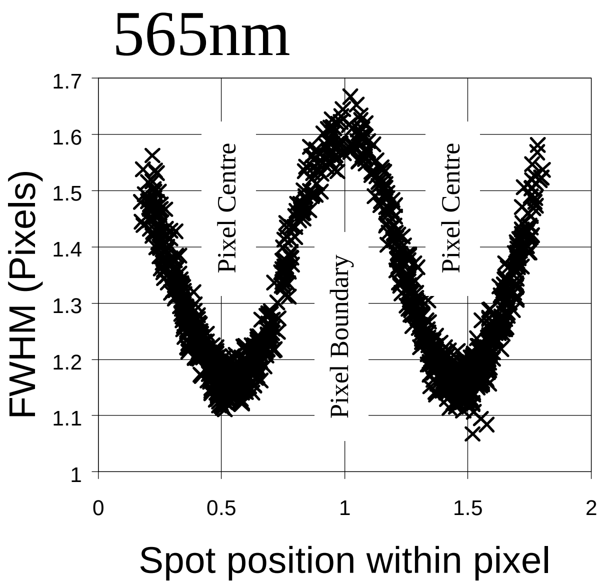


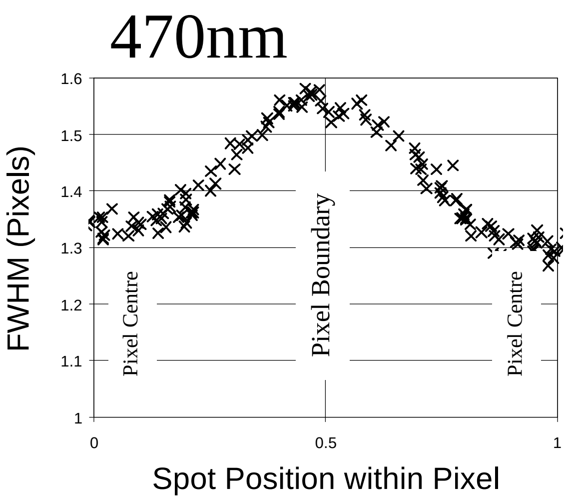


3.4. Point Spread Function.

This was measured at two wavelengths using an optical device developed at RGO. This device used an all reflective microscope objective, pinhole and LED to project a 2μm diameter spot onto the CCD. The position of this spot could be adjusted to high precision using an X-Y translation stage. Focusing was achieved by tilting the CCD slightly with respect to the X-Y plane in which the scan head moved. The spot was then scanned down a column of the CCD during integration , thus drawing out a line image. As the spot moved first towards and then away from best focus, the width of this scan line could be seen to reach a minimum. It was thus possible to window in on a few hundred image rows close to this minimum where optimum focus was to be found. The X and Y axes of the translation stages were only approximately aligned to the rows and columns of the CCD. As the line image was scanned out down a column, there would therefore be a small component of motion along the row axis of the chip. By examining consecutive rows of the line image (close to the optimum focus position) it was then possible to measure the optical properties of the CCD at differing intra-pixel spot positions. Each line image therefore contained a great deal of information. An alternative, and very much more complex method would be to record several hundred individual spot images, stepping the position of the spot very slightly between each.

Line images were recorded at two wavelengths and the results are shown below. The CCD showed excellent spatial resolution, at least compared to Lesser thinned Loral devices.





4. Readout Noise and Readout Times

This was measured comprehensively using both photon-transfer image pairs and the more accurate Iron-55 X-ray method.

Performance of Left Hand Amplifier in Hi-Gain mode (Fe55 Method)

speed	Gain (e/ADU)	Noise (e)	Bias (ADU)
S	1.13	3.9	1900
Q	1.26	4.6	1590
T	1.56	5.2	1030
N	1.84	5.0	700

Performance of Right Hand Amplifier in Hi-Gain mode (Photon Transfer)

speed	Gain (e/ADU)	Noise (e)	Bias (ADU)
S	1.1	5	2000
Q	1.2	5	1700
T	1.5	5.6	1100
N	1.9	5.2	750

Performance of Left Hand Amplifier in Lo-Gain mode (Fe55 Method)

speed	Gain (e/ADU)	Noise (e)	Bias (ADU)
S	3.05	10.2	1900
Q	3.43	12.5	1600
T	4.16	14.3	1050
N	5.01	13.1	700

Performance of Right Hand Amplifier in Lo-Gain mode (Photon Transfer)

speed	Gain (e/ADU)	Noise (e)	Bias (ADU)
S	3.0	11.5	2020
Q	3.6	13.5	1700
T	4.4	15	1110
N	5.2	14.5	760

Binned Performance of Left Hand Amplifier in Hi-Gain Mode(Fe55 Method)

Binning	Gain (e/ADU)	Noise (e)	Bias (ADU)
2x2	1.60	5.2	1510
1x2	1.53	5.4	1870
2x1	1.60	5.6	1510

Readout Times

Speed	Full frame readout (s)
S	225
Q	180
T	165
N	120
2x2 Bin	47

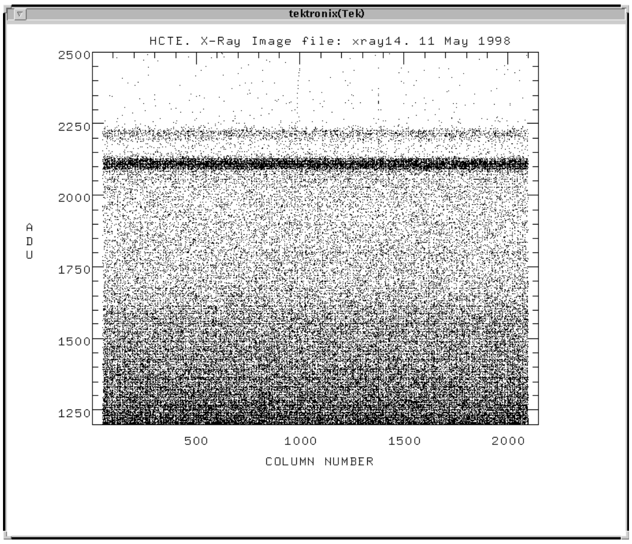
5. Charge Transfer Efficiency.

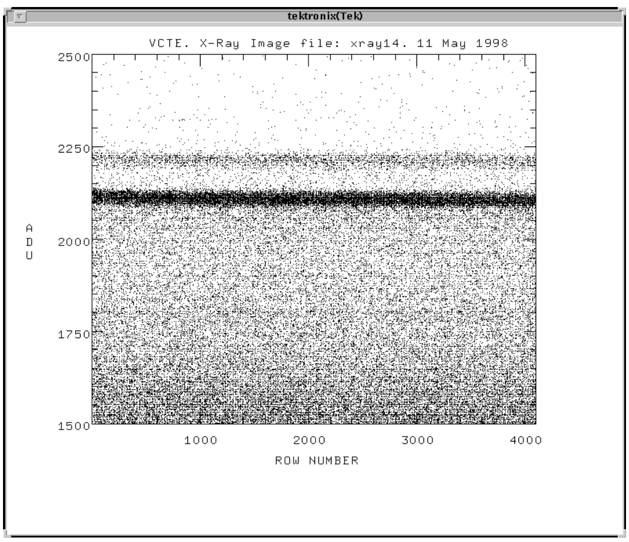
This was measured for low charge levels (1620e$^-$) using Iron-55 X-rays, and for higher levels close to full-well, using the Extended Pixel Edge Response technique. The results are tabulated below.

VCTE Fe55 (1620e$^-$)	0.999998
HCTE Fe55 (1620e$^-$)	0.999998
VCTE 200,000e$^-$	0.999997
HCTE 200,000e$^-$	0.9999987

Measurement temperature=-120C

Plots of the x-ray event pixel values along the horizontal and vertical image axes are shown below.

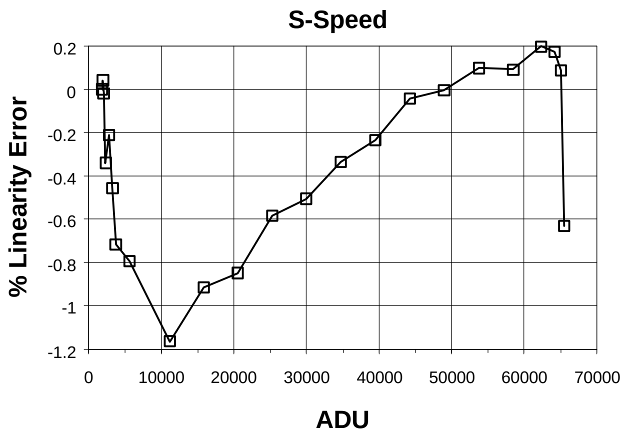


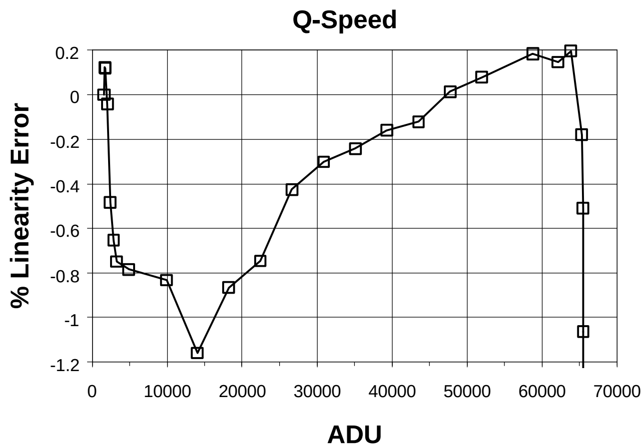


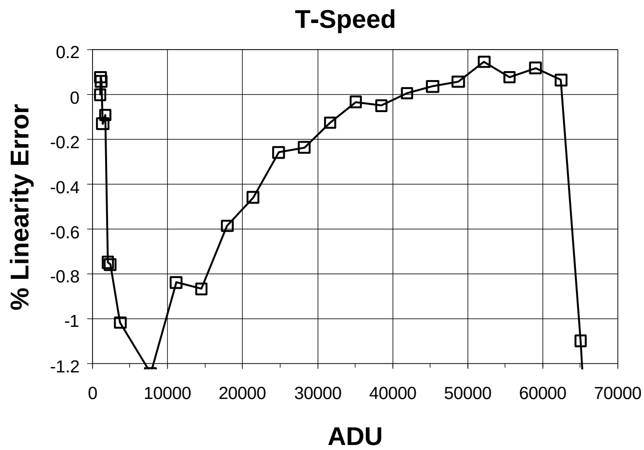
6. Linearity and Full-Well.

These characteristics were measured using a highly linear pulsed light source developed at RGO.

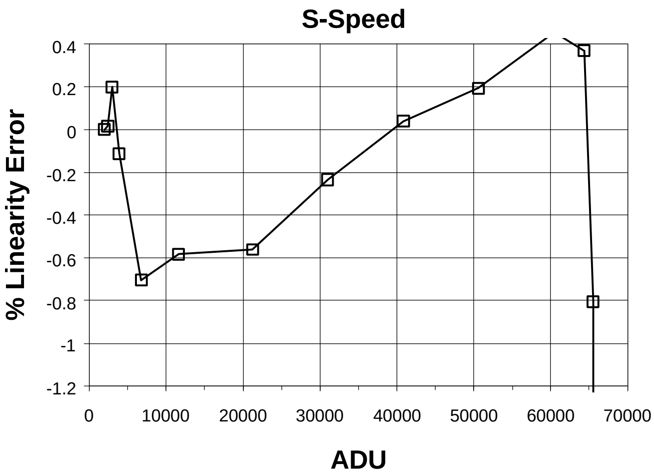
Hi-Gain Mode Linearity
LEFT Hand Output

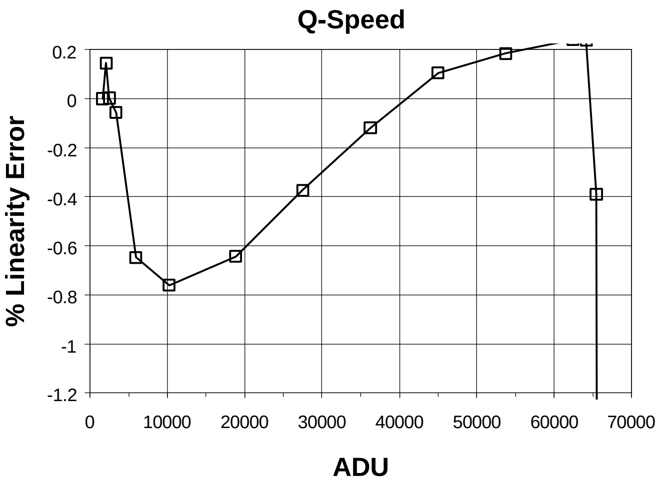


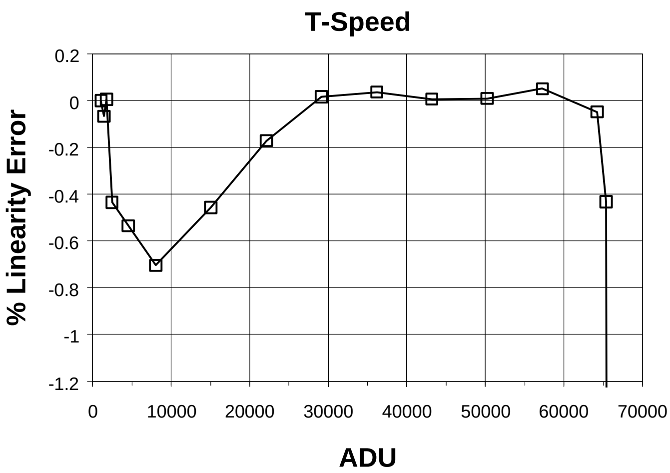




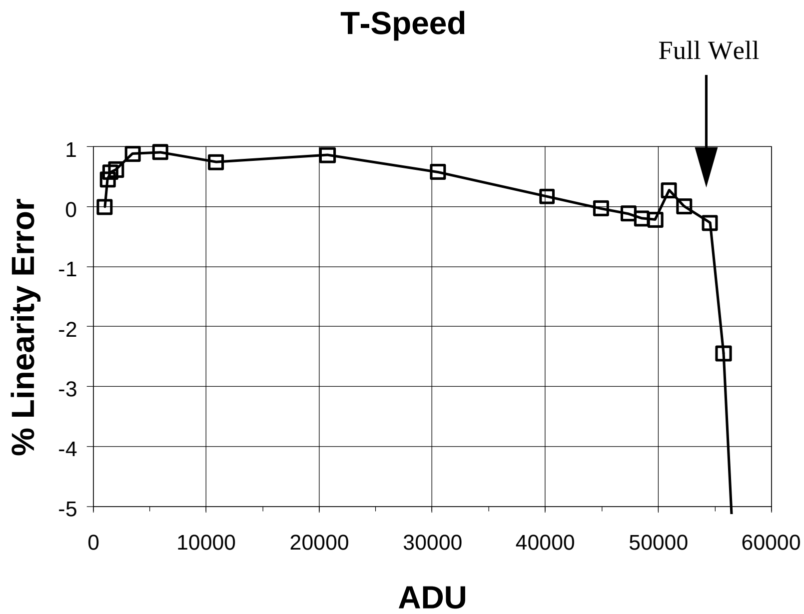
Hi-Gain Mode Linearity
RIGHT Hand Output

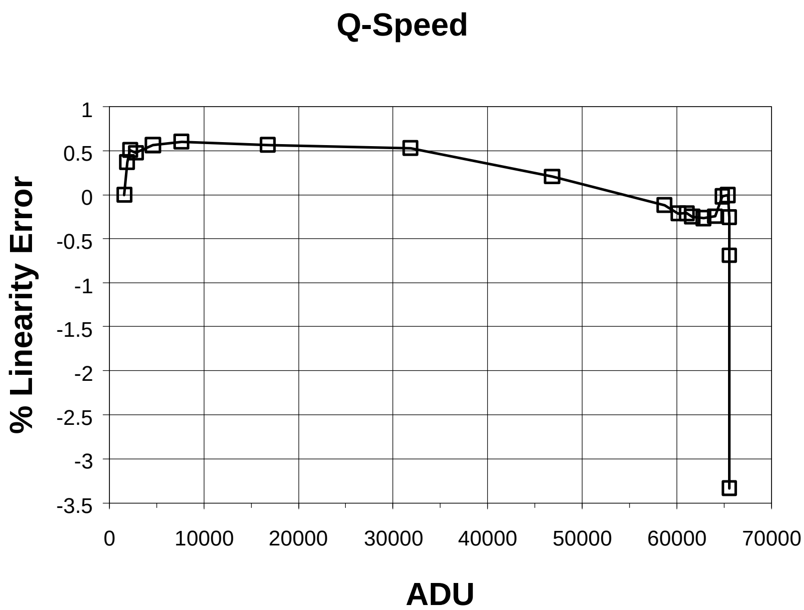




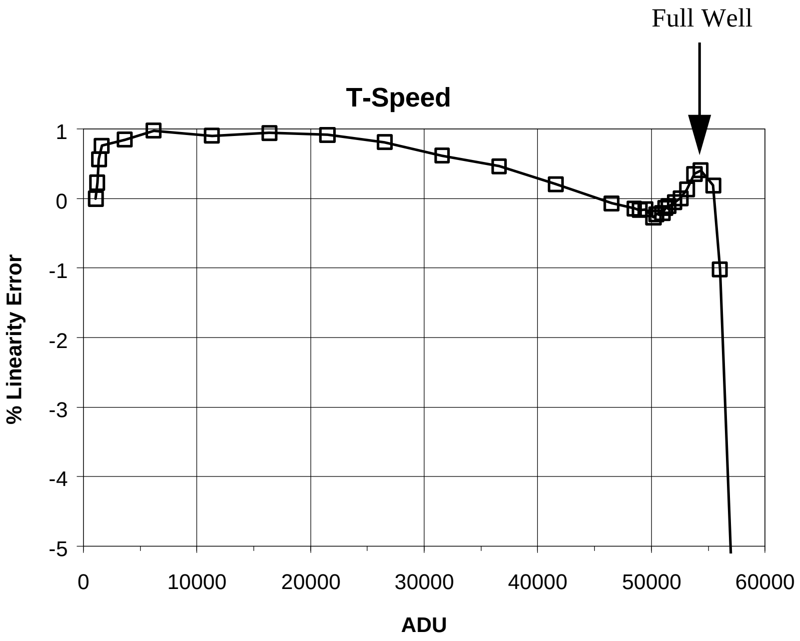


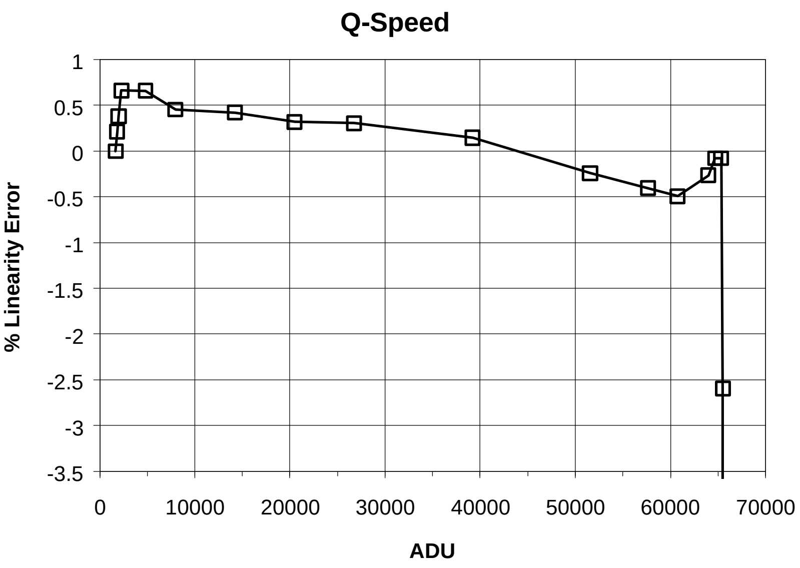
Lo-Gain Mode Linearity
LEFT Hand Output



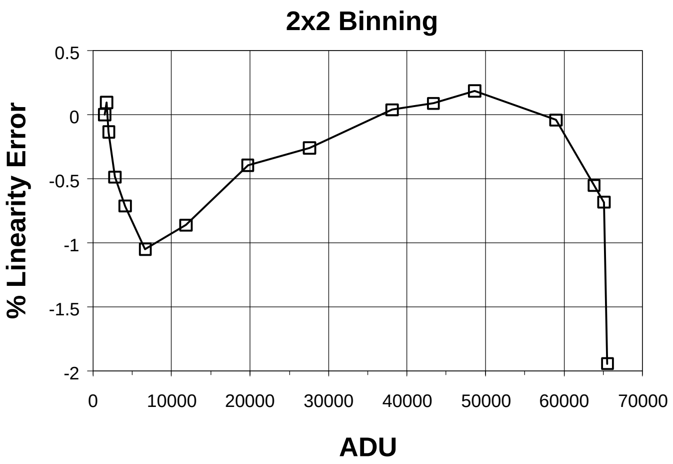


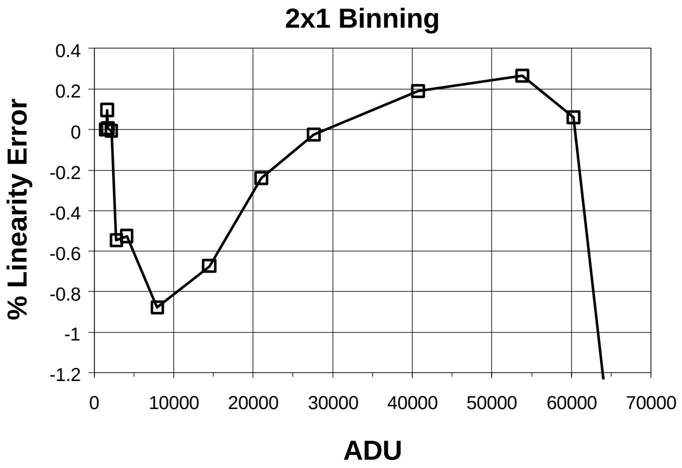
Lo-Gain Mode Linearity
RIGHT Hand Output

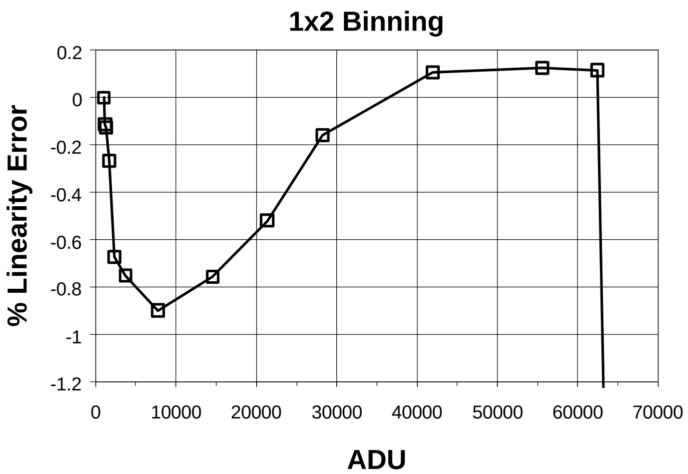




Binning Mode Linearity
LEFT Hand Output, Hi-gain





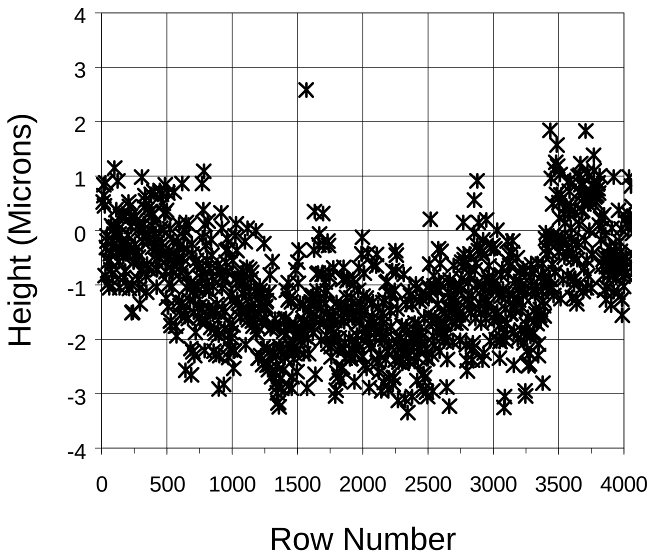


7. Mechanical Parameters.

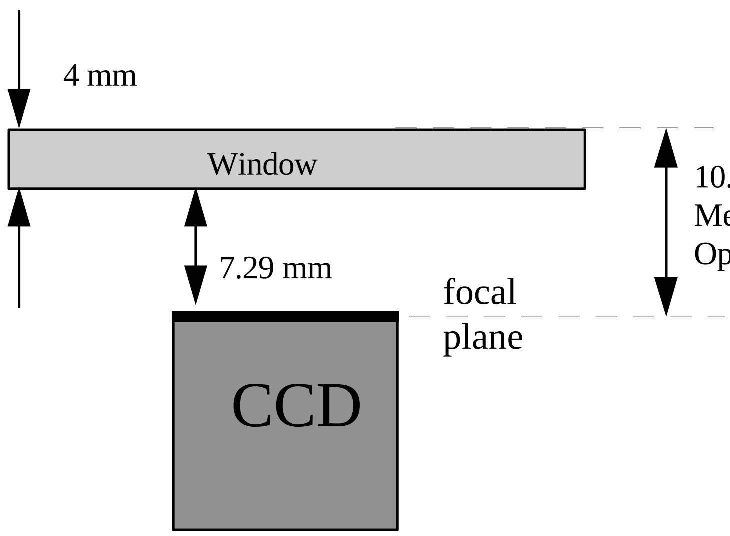
The flatness of the CCD was measured using the RGO coplanarity scanner. The distance of the CCD behind the cryostat window was measured using a travelling microscope.

7.1. Device Flatness.

The CCD was extremely flat. The following plot shows a height data from a measurement scan down the long axis of the CCD close to the central column.



7.2. Focus Distance.



Appendix A. CCD Controller Configuration Listing.

```
xterm
  1   RAM-DISK 0
( DEFINE CLOCKS     ) SEQUENCER DEFINITIONS (          05 May 98)
\  For EEV 42-80 op(L)
00  0 CLOCK  TRACK    ( TS0 )   01  1 CLOCK  TRIG     ( AC0 )
02  0 CLOCK  SIG-SAMP ( CS0 )   03  0 CLOCK  REF-SAMP ( CR0 )
04  1 CLOCK  SIG-RST  ( RS0 )   11  1 CLOCK  REF-RST  ( RR0 )
17  1 CLOCK  CLAMP    ( CL0 )   25  0 CLOCK  RSCK     ( RSA )
( HA1) 23  1 CLOCK  1HCK  \ 23 op(L) 30 op(R)
( HA2) 30  0 CLOCK  2HCK  \ 30       23
( HA3) 34  0 CLOCK  3HCK
( HA4) 28  0 CLOCK  SWCK
( VA1) 24  0 CLOCK  1VCK  \ lower reg. only for 42 series
( VA2) 26  1 CLOCK  2VCK
( VA3) 19  0 CLOCK  3VCK
( VA4) 31  0 CLOCK  4VCK  \ used for DG
( VLA) 35  0 CLOCK  RD/I  \ was 0,  27/11
 -->
<CCD7> ok
```

```
xterm
  2   RAM-DISK 0
( Vertical clock ) SEQUENCER DEFINITIONS      (  apo 18 Dec 97)
0 SOR  VCLOCK
\              RD/I  650  ND
               1VCK  300  DF  300  ND    \  1VCK 300+300
\              1VCK  200  DF  300  ND    \  1VCK 300+300
               2VCK  200  DF  300  ND    \       200+300
\              2VCK  100  DF  300  ND    \       200+300
               3VCK  100  DF  300  ND    \  3VCK 100+300
\              3VCK  300  DF  300  ND    \  3VCK 100+300
               2HCK  950  ND      \ 650  2clks hi during v->h
1000  EOR                              \ 700, 1000
VCLOCK >RAM
-->



<CCD7> ok
```

```
xterm
  3   RAM-DISK 0
( Horizontal clock ) SEQUENCER                  (  smt 13 May 98)
1 SOR HCLOCK
             RSCK 10 DF 20 ND
             1HCK  5 DF 15 ND
             2HCK 15 ND
             3HCK 10 DF 15 ND
             SWCK 10 DF 15 ND
35 EOR       HCLOCK >RAM

15  SOR      HRINT           \ clock serial reg to remove glow
             RSCK   25 ND
             1HCK   5 DF 15 ND
             2HCK   15 ND
             3HCK   10 DF 15 ND
             4VCK   1000 ND
1001 EOR     HRINT >RAM          -->
<CCD7> ok
```

xterm

```
  4   RAM-DISK 0
                                                ( SMT 11 May 93)
      8 SOR ABM-CLK      ( WOBBLE 1->2->1 )
     RD/I 32000 ND
     RSCK 32000 ND
     1HCK 32000 ND
     2HCK 32000 DF
     3HCK 32000 ND
     1VCK  4000 DF 8000 ND
     2VCK  6000 DF 4000 ND
 \   3VCK  32000 ND
 \   4VCK  32000 ND
 32002 EOR ABM-CLK >RAM -->




<CCD7> ok
```

xterm

```
  5   RAM-DISK 0
                                                  ( smt 13 May 98)
 13 SOR REM-CLK

    1VCK  5000 DF
    2VCK  5000 ND
    3VCK  5000 DF
    1HCK  5000 ND



    5002 EOR REM-CLK >RAM




 -->
<CCD7> ok
```

xterm

```
  6   RAM-DISK 0
 (                                                 SMT 28 Apr 93)









 BLK  @  1+ VHT BIN-BLOCK !
 6 SOR BIN
   3 FH LOAD



<CCD7> ok
```

xterm

```
  7   RAM-DISK 0
( Binned Block - 1   ) DECIMAL    (              smt 06 May 98)
SEQUENCER VIA SEQUENCER FORTH ENDVIA  DEFINITIONS
: COMPILE-BIN-PIX ( xbin-factor -- )      >R  BIN SOR
    RSCK   15 ND
    1HCK    5 DF  I 0 DO    5 DF 15 ND  5 DF  LOOP
    2HCK    5 ND  I 0 DO   15 ND 10 DF        LOOP
    3HCK    5 DF  I 0 DO    5 DF 15 ND  5 DF  LOOP
    [
-->
<CCD7> ok
```

xterm

```
  8   RAM-DISK 0
( Binning Block - 2    ) DECIMAL         (        smt 06 May 98)
    ]
    REF-SAMP    5 DF   I 25 * DF   5 DF  40 ND
    SWCK        5 DF   I 25 * ND  55 ND  10 DF 65 ND
    SIG-SAMP    5 DF   I 25 * DF  80 DF  40 ND
    CLAMP       5 DF   I 25 * DF 5 DF 125 ND
    SIG-RST     5 DF   I 25 * DF 5 DF 125 ND
    REF-RST     5 DF   I 25 * DF 5 DF 125 ND
    TRACK       5 DF   I 25 * DF  80 DF 45 ND
    TRIG        5 DF   I 25 * DF 125 DF  5 ND
 R> 25 * 135 +  EOR  BIN >RAM  ;
COMPILE-BIN-PIX BIN-TEMP  FORGET COMPILE-BIN-PIX
<CCD7> ok
```

xterm

```
  9   RAM-DISK 0
( Standard readout speed )        SEQUENCER (     smt 29 Apr 98)
2 SOR SP0   ( 8+8 us, 190s for whole frame )
  RSCK       13 ND
  1HCK        5 DF   15 ND
  2HCK       15 ND
  3HCK        5 DF   15 ND
  REF-SAMP   25 DF   80 ND
  SWCK       10 DF  105 ND  10 DF 110 ND
  SIG-SAMP  135 DF   80 ND
  TRACK     135 DF   85 ND
  TRIG      230 DF    5 ND
  CLAMP      25 DF  210 ND
  SIG-RST    25 DF  210 ND
  REF-RST    25 DF  210 ND
236 EOR     SP0 >RAM  -->
<CCD7> ok
```

xterm

```
   10   RAM-DISK 0
 0 ( QUICK  readout speed )          SEQUENCER (     smt 11 May 98)
 1 3 SOR SP1    ( 6+6us  160s readout     )
 2    RSCK        13 ND
 3    1HCK         5 DF   15 ND
 4    2HCK        15 ND
 5    3HCK         5 DF   15 ND
 6    REF-SAMP    25 DF   60 ND
 7    SWCK        10 DF   85 ND  10 DF 90 ND
 8    SIG-SAMP   115 DF   60 ND
 9    TRACK      115 DF   65 ND
10    TRIG       190 DF    5 ND
11    CLAMP       25 DF  170 ND
12    SIG-RST     25 DF  170 ND
13    REF-RST     25 DF  170 ND
14
15 196 EOR     SP1 >RAM  -->
<CCD7> ok
```

xterm

```
   11   RAM-DISK 0
 0 ( TURBO readout speed )    SEQUENCER        (     smt 11 May 98)
 1 4 SOR SP2    ( 4.0 + 4.0 us CDS, 140s readout )
 2    RSCK        13 ND
 3    1HCK         5 DF   15 ND
 4    2HCK        15 ND
 5    3HCK         5 DF   15 ND
 6    REF-SAMP    23 DF   40 ND
 7    SWCK         5 DF   68 ND  10 DF 75 ND
 8    SIG-SAMP    98 DF   40 ND
 9    TRACK       98 DF   45 ND
10    TRIG       153 DF    5 ND
11    CLAMP       23 DF  135 ND
12    SIG-RST     23 DF  135 ND
13    REF-RST     23 DF  135 ND
14
15 179 EOR     SP2 >RAM  -->
<CCD7> ok
```

xterm

```
   12   RAM-DISK 0
 0 ( Nonastro readout speed )          SEQUENCER (   smt 11 May 98)
 1  5 SOR SP3    ( 3 + 3 us, 93s readout )                  )
 2    RSCK        13 ND
 3    1HCK         5 DF   15 ND
 4    2HCK        15 ND
 5    3HCK         5 DF   15 ND
 6    REF-SAMP    25 DF   30 ND
 7    SWCK         5 DF   60 ND   8 DF 53 ND
 8    SIG-SAMP    83 DF   30 ND
 9    TRACK       83 DF   35 ND
10    TRIG       123 DF    4 ND
11    CLAMP       25 DF  100 ND
12    SIG-RST     25 DF  100 ND
13    REF-RST     25 DF  100 ND
14
15  128 EOR     SP3 >RAM  -->
<CCD7> ok
```

xterm

```
  13   RAM-DISK 0
( Dummy pixel routine     )           SEQUENCER (    SMT 28 Apr 93)
14 SOR DPIX    ( ***** DUMMY PIXEL 1+1us CDS )
   RSCK       13 ND
   1HCK        4 DF    10 ND
   2HCK        9 ND
   3HCK        4 DF    10 ND
   REF-SAMP   18 DF    10 ND
   SWCK        5 DF    26 ND    8 DF 35 ND
   SIG-SAMP   44 DF    10 ND
\  TRACK      44 DF    15 ND       \ NO A/D or S/H trig for dummy
\  TRIG       64 DF     4 ND
   CLAMP      15 DF    59 ND
   SIG-RST    15 DF    59 ND
   REF-RST    15 DF    59 ND

75  EOR     DPIX >RAM  -->
<CCD7> ok
```

xterm

```
  14   RAM-DISK 0
( Vmov w/o SR scan        ) SEQUENCER       (      smt 11 May 98)
 6 SOR QUICK-CLR

              1VCK 150 DF 150 ND
              2VCK 100 DF 150 ND
              3VCK  50 DF 150 ND


              1HCK 400 ND
              2HCK 400 DF
              3HCK 400 DF
400 EOR
QUICK-CLR   >RAM
\ V-clock charge into last row(s) to overcome low CTE...
-->

<CCD7> ok
```

xterm

```
  15   RAM-DISK 0
( Flash fast clear of CCD ) SEQUENCER       (      apo 27 Jan 97)
 7 SOR FLASH-CLR
\             RD/I 350 ND
              1VCK 150 DF 150 ND
              2VCK 100 DF 150 ND
              3VCK  50 DF 150 ND
              4VCK 400 ND      \ This manipulates DD on the EEV
\             RSCK 400 ND
              1HCK 400 DF
              2HCK 400 ND
              3HCK 400 ND
410 EOR
FLASH-CLR   >RAM
\ 1 V-clock triplet then dump into register drain x n for EEV4x
-->

<CCD7> ok
```

```
xterm
  16   RAM-DISK 0
 0  ( SETUP FUNCTIONS.                                     smt 11 May 98)
 1 SP0                   SET-SPEED0
 2 SP1                   SET-SPEED1
 3 SP2                   SET-SPEED2
 4 SP3                   SET-SPEED3
 5 SP0                   SET-SPEED4
 6 BIN                   SET-BIN
 7 HCLOCK                SET-DPIX
 8 HCLOCK                SET-HCLK
 9 VCLOCK                SET-VCLK
10 HRINT                 SET-HIDLE
11 QUICK-CLR             SET-QCLR
12 ABM-CLK               SET-AB   \ ANTI-BLOOM
13 REM-CLK               SET-RR   \ ANTI-REMNANCE
14 \                     SET-CLKT
15 FLASH-CLR             SET-FCLR     -->
<CCD7> ok
```

```
xterm
  17   RAM-DISK 0
 0 ( Customisations for EEV42) FORTH DEFINITIONS (    smt 13 May 98)
 1 : PFS   PREFLASH-SCALER ;  40   PFS !    \ 1 unit = 1.25us
 2 : ENBT 0 'SILENT C!  VT100   RAM-DISK   1   LIST
 3                 ( [ CCDS ] CONFIG ) ;
 4 : S-CLR [ VHT ] STANDARD CLEAR-SPEED ;
 5 : Q-CLR [ VHT ] QUICK     CLEAR-SPEED ;
 6 : F-CLR [ VHT ] FLASH-CLR CLEAR-SPEED ;
 7 : IOS  1 ?IS ;  : SETI  -1 TIMES  IOS  ;
 8 1 VHT 'REM-REMO C! 3000 RR-CLKS ! \ ENABLE REMNANCE
 9 : HOPG  2 OPG  ;    : LOPG  1 OPG ;
10 : VMOV  [ SEQUENCER ] HERE 4096 3 FC HERE >FIFO     ;
11     1V  2148 4128 13 NEW-TYPE  EEV48    EEV48
12 0 VHT 'ANTI-BLOOM C!              \ DISABLE ANTI-BLOOM
13 \   Attributes are   3      2      1      0
14 \                   dump-   opg-   no-    od-sw
15 -->    \           drain    sw    idle
<CCD7> ok
```

```
xterm
  18   RAM-DISK 0
 0 ( Customisations - general) SEQUENCER    (            11 May 98)
 1 5 [ ' ] PA-RES !                   \ P/A res = 470ohms
 2  1 1 I-OFFSET ! 7 2 I-OFFSET !  \ Set ?IS offset, for 2 heads
 3  38 1 OD-ZERO ! 40 2 OD-ZERO !  \ OD Offset. For 2 heads
 4 1 PHYSICAL    2064 'ZERO-AD !    0 'SERVO-ZERO !
 5 2 PHYSICAL    2064 'ZERO-AD !    0 'SERVO-ZERO !
 6 FORTH DEFINITIONS
 7
 8 1P -15 'SERVO-ZERO !   T-ON     \ 1 unit = -0.16 degC
 9 98 YEAR W!
10 NETWORK CCD7
11 : WHO? PAGE BELL  CR  20 SPACES  ." EEV 4280     " CR ;
12 : OPGH 0 OPG ;    : OPGL  1 OPG ;
13
14 WHO?   -->
15
<CCD7> ok
```

Appendix B. Hardware Modifications to CCD Controller.

The CDS time constant was set to 4µs . This was achieved by setting C8 and C7 =6.6nF and R12 and R13 =620 Ohms. R5 on the CDS card was set to 50K. Pre-amp resistors R31,32,33,34 all had 4K7 resistors soldered in parallel to reduce gain. The corresponding electronic gain of the controller is as follows :

Readout Speed	Voltage Gain
S	29.8
Q	26.9
T	21.6
N	18.3

Appendix C. Operating Voltages.

```
xterm

                    Chip 0 Configuration.
    Virtual head number 1      Serial number is :- EEV42-80, A5500-5

  0       0.00 Volts  Channel   0         1       0.00 Volts  Channel   0
  2       0.00 Volts  Channel   0         3       0.00 Volts  Channel   0
  4       0.00 Volts  Channel   0         5       0.00 Volts  Channel   0
  6       0.00 Volts  Channel   0         7       0.00 Volts  Channel   0
 V+SL   -17.70 Volts  Channel   8        V-     -16.00 Volts  Channel   9
 V+      -6.50 Volts  Channel  10        V-SL     2.40 Volts  Channel  11
 RD       4.00 Volts  Channel  12        VSS     -9.00 Volts  Channel  13
 OG1    -13.00 Volts  Channel  14        V++     -6.50 Volts  Channel  15
 R-SL     2.00 Volts  Channel  16        R-     -15.00 Volts  Channel  17
 R+      -5.00 Volts  Channel  18        R+SL   -18.00 Volts  Channel  19
 ODL      7.00 Volts  Channel  20        ODH     16.50 Volts  Channel  21
 OG2H   -12.00 Volts  Channel  22        OG2L     3.00 Volts  Channel  23
 24       0.00 Volts  Channel   0        BG       7.00 Volts  Channel  25
 DMP      5.00 Volts  Channel  26        H++     -2.00 Volts  Channel  27
 H+      -5.00 Volts  Channel  28        H-     -14.00 Volts  Channel  29
 H-SL     2.00 Volts  Channel  30        H+SL   -18.00 Volts  Channel  31

<CCD7> ok
█
```