Rate Generator RGB1880

Original Marconi Ref: L-41-0607

General

The rate generator board is contained within the Servo Rack SCR1884 and forms the rate generator module. The function of the rate generator board is to provide a serial pulse stream at a frequency which is a function of the main clock frequency and a parallel word of 15bits provided by the R.G.O. computer via the CAMAC crate CU1955. This serial pulse stream represents the rate demand for the particular channel of the telescope drive in which the board is located.

In addition, the incremental encoder feedback signal for the channel is received by the rate generator board and is processed to provide a serial pulse stream of a frequency equal to the actual rate of the encoder and also a direction signal representing the actual direction of the encoder.

Description

The CAMAC signals received from the OR/48 drive module are open collector, negative logic. These signals are interfaced by IC's 3, 4 and 5 and are latched onto the board by IC's 8, 9 and 10. The latches are clocked by a positive going strobe pulse from the CAMAC crate.

The 15bit rate demand is input, along with the 1MHz system clock, to three rate generators, IC's 12, 13 and 14, the outputs of which are serial pulse streams. These three serial signals are combined by IC16a and fed to the 'down' input of IC18 which forms the first stage a cascaded 'programmable' divider formed by IC's 18, 19 and 20. The divider is required since each channel of the telescope drive system require different rate demands in relation to the main clock frequency of 1 MHz. At the end of each successive count cycle a 'load' signal is generated to reset the divider. The load signal is derived at IC16b by gating the rate signal from IC16a, with the output of the divider IC1p8. The 'load' signal is also gated with the CAMAC clear signal by IC21a, so producing a divider 'reset' if either signal is asserted. Switches SW1, 2 and 3 are used to program the divider.

The output of the divider, IC1p8, is also input to a 'D' type flip-flop, IC22, used to synchronise the rate demand pulse stream with the **ϕ_2 clock** and prevent coincidence with the encoder rate pulse stream which is synchronised to the ϕ_1 clock.

The incremental encoder feedback signals are received by IC's 2 and 6, IC11 selects one of two encoder signals, the selection being determined by a signal from the CAMAC crate. IC's 15 and 17 produce a direction signal dependent on the encoder feedback signal, i.e. it will be either a clockwise or a counter-clockwise signal. The encoder rate signal is passed through a gated delay, IC7, to ensure that the direction signal is received by the direction processing circuit (on Counter pcb CTB1881) before the rate pulse. The encoder rate pulse stream is input to IC23 and sychronised with the **ϕ_1 clock** to prevent coincidence with the rate demand signal.

Calculation of the Rate Demand output frequency is obtained from the rate output frequency of the binary multiplier divided by the ratio of the programmable counter....

$$f_{dem} = f_{mult} / (N + 1)$$

where..... N is the divide ratio set by switches SW1, SW2, SW3.
f_{mult} is the out frquency of the binary multiplier.

The frequency output from a **single** SN7497 binary rate multiplier is given by:

$$f_{mult} = \frac{M \times f_{in}}{64}$$

where.... f_{in} is the clock frequency (1 MHz)
M is the rate input, given by.....
$M = (F \times 2^5) + (E + 2^4) + (D \times 2^3) + (C + 2^2) + (B \times 2^1) + (A \times 2^0)$
A to F are rate generator inputs to a SN7497 binary rate multiplier IC, the rate inputs being active high.

Similarly the frequency output from the **3 cascaded** binary rate multiplier, IC's 12, 13 and 14 (connected to give 15bit rate multiplication) is given by:

where $M = \overset{b14}{(F_3 \times 2^5)} + \overset{b13}{(E_3 \times 2^4)} + \overset{b12}{(D_3 \times 2^3)} + \overset{b11}{(C_3 + 2^2)} + \overset{b10}{(B_3 \times 2^1)} + \overset{b9}{(A_3 \times 2^0)}$

$+ \overset{b8}{(F_2 \times 2^{-1})} + \overset{b7}{(E_2 \times 2^{-2})} + \overset{b6}{(D_2 \times 2^{-3})} + \overset{b5}{(C_2 + 2^{-4})} + \overset{b4}{(B_2 \times 2^{-5})} + \overset{b3}{(A_2 \times 2^{-6})}$

$+ \overset{b2}{(F_1 \times 2^{-7})} + \overset{b1}{(E_1 \times 2^{-8})} + \overset{b0}{(D_1 \times 2^{-9})}$...*($C_1$, B_1 and A_1 not used)*

i.e. each term represents a binary input to the rate multiplier.

e.g. given an input word of 1008 (hex) .....

Then the multiplier output frequency would be .....

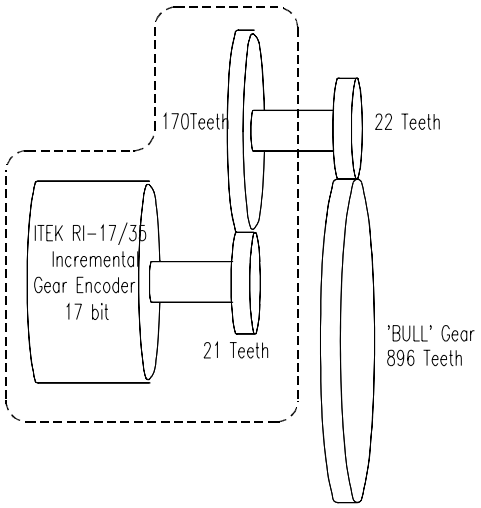
$$f_{mult} = \frac{[2^3 + 2^{-6}] \times (1Mhz)}{64} = \frac{8.0156 \times 1 \times 10^6}{64} \qquad f_{mult} = 125.06KHz$$

The maximum frequency is of course determined by the system clock i.e. .....

$$\frac{[2^5 + 2^4 \ldots\ldots 2^{-9}] \times 1Mhz}{64} = \frac{[64] \times 1Mhz}{64} = 1Mhz$$

The division ratio of the divider circuit is determined by the maximum rate of encoder pulses generated from the incremental encoder for each drive system, i.e. the division ratio sets the maximum demanded rate frequency to be the same as the maximum velocity (1deg/sec) of the driven device . The actual rate demand maximum should be capable of just exceeding the maximum velocity to permit a small 'overhead' for servoing at the velocity limit. Calculation of the ratios for each of the drives is illustrated below.....

Elevation and Azimuth



Encoder = 2^{17} bits/rev (131,072)

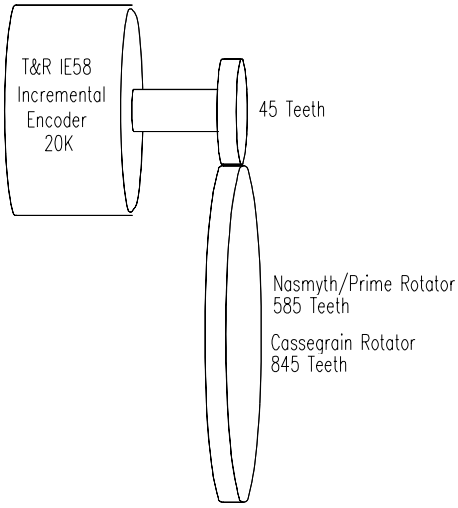
Gear ratio = $\frac{896}{22} \times \frac{170}{21} = 329.7$

Bits per degree = $\frac{2^{17} \times 329.7}{360} = 120{,}040.1$

Divider ratio = $\frac{10^6}{120{,}040.1} = \mathbf{8}$ (rounded down)

also divider ratio = N+1 $\therefore$ **N = 7**

Similarly, the values for the rotators are obtained using the encoder and gear ratio's for the particular drive. The Cassegrain, Nasmyth and Prime rotator systems all use the same incremental encoder, the Nasmyth and Prime also have identical gears, so the theoretical divider values are....



Cassegrain

Encoder = 20k bits/rev

Gear ratio = $\frac{845}{45} = 18.77$

Bits per degree = $\frac{20K \times 18.77}{360} = 1043.2$

Divider ratio = $\frac{10^6}{1043.2} = \mathbf{958.6}$

note: Actual value for Cassegrain used by Marconi is 801 which is equivalent to 1.19 degs/sec

Prime/Nasmyth

Gear ratio = $\frac{585}{45} = 13$

Bits per degree = $\frac{20K \times 13}{360} = 722.22$

Divider ratio = $\frac{10^6}{722.22} = \mathbf{1384.6}$

note: Actual for Prime/Nasmyth used by Marconi is 1164 which is also equivalent to 1.19 degs/sec.

The Azimuth Inductosyn Tape Encoder also has to be accommodated with the new Marconi system, the higher resolution of the tape system being the principle reason for increasing the frequency of the sampling clocks (ϕ_1 and ϕ_2) from 1MHz to 4MHz.

Tape resolution and Maximum pulse rate

The tape pitch is 2mm, each pitch is electronically interpolated by a factor of 2^{14}. The overall length of the tape is defined by the ∅6064mm diameter of the tape mounting surface, therefore the tape resolution and pulse rate is.....

tape length = Circumference of mount surface = πD
= π x 6064
= 19050mm

pulse rate = $\frac{\text{tape length x } 2^{14}}{\text{tape pitch x } 360}$ $\frac{19050 \text{ x } 2^{14}}{2 \text{ x } 360}$ = 433,493.33 bits/deg

and resolution = $\frac{3600}{433,493.33}$ = 0.0083 arc seconds/bit

Assuming a 20% overhead on the rate demand to permit servoing at 1deg/sec then the max rate demand will be .....

$$f_{maxdem} = 1.2_{(deg/sec)} \text{ x } 433,493.33_{(bits/deg)} \cong 520,192 \text{ Hz}$$

and Divider ratio = $\frac{10^6}{520,192}$ = 1.922 *(min available = 2)*

However the divider circuit is constrained to a minimum divide ratio of 2, so .....

Actual rate maximum = $\frac{433,493.33}{(10^6/2)}$ = 1.15 deg/s

Rate Switch Settings
The divider ratios are selected using SW1, SW2 and SW3. Each switch provides a 4 bit code used to pre-set the counter (IC18,19&20). The programmed count value determines the rate demand division ratio....

Dision ratio = N+1 (where N is the count magnitude.)

and Rate demand f_{dem} = $\frac{f_{mult}}{(N + 1)}$

The table below represents the switch positions on the PCB to give the binary divide ratio for 'N'. A logical '0' is generated when the switch is 'on', i.e. contacts are 'made', conversely a logical '1' is generated when the switch is in the off position and the contacts are open....

	SW3(MSW)	SW2	SW1(LSW)	Hex
	b11 b10 b9 b8	b7 b6 b5 b4	b3 b2 b1 b0	
AZ Tape off (1)	- - - -	- - - -	- - - ↓	
on (0)	↓ ↓ ↓ ↓	↓ ↓ ↓ ↓	↓ ↓ ↓ -	**001_H**
AZ/ALT off (1)	- - - -	- - - -	- ↓ ↓ ↓	
on (0)	↓ ↓ ↓ ↓	↓ ↓ ↓ ↓	↓ - - -	**007_H**
CASS.TT off (1)	- - ↓ ↓	- - ↓ -	- - - -	
on (0)	↓ ↓ - -	↓ ↓ - ↓	↓ ↓ ↓ ↓	**320_H**
PFTT/NAS off (1)	- ↓ - -	↓ - - -	↓ - ↓ ↓	
on (0)	↓ - ↓ ↓	- ↓ ↓ ↓	- ↓ - -	**$48B_H$**

The switches, when viewed on the PCB with SW1 to the right appear as above and the 12bit binary code can easily be read. The switch readings are shown below for clarity with the calculations for the maximum rate demand.

Azimuth Tape:

0000 0000 0001 = 1_{HEX} = 1

$$f_{maxdem} = \frac{10^6}{(1+1)} = 500{,}000 \text{ Hz or } 1.15 \text{ degs/sec } (@433{,}493.33 \text{ bits/deg})$$

Azimuth and Elevation:

(SW3) (SW2) (SW1)

N = 0000 0000 0111 = 007_{HEX}

$$f_{maxdem} = \frac{10^6}{(7+1)} = 125{,}000.0 \text{ Hz or } 1.04 \text{ degs/sec } (@120{,}040.1 \text{ bits/deg})$$

Cassegrain rotator:

0011 0010 0000 m 320_{HEX} = 800

$$f_{maxdem} = \frac{10^6}{(800+1)} = 1248.4 \text{ Hz or } 1.19 \text{ degs/sec } (@ 1043.2 \text{ bits/deg})$$

Prime/Nasmyth rotator:

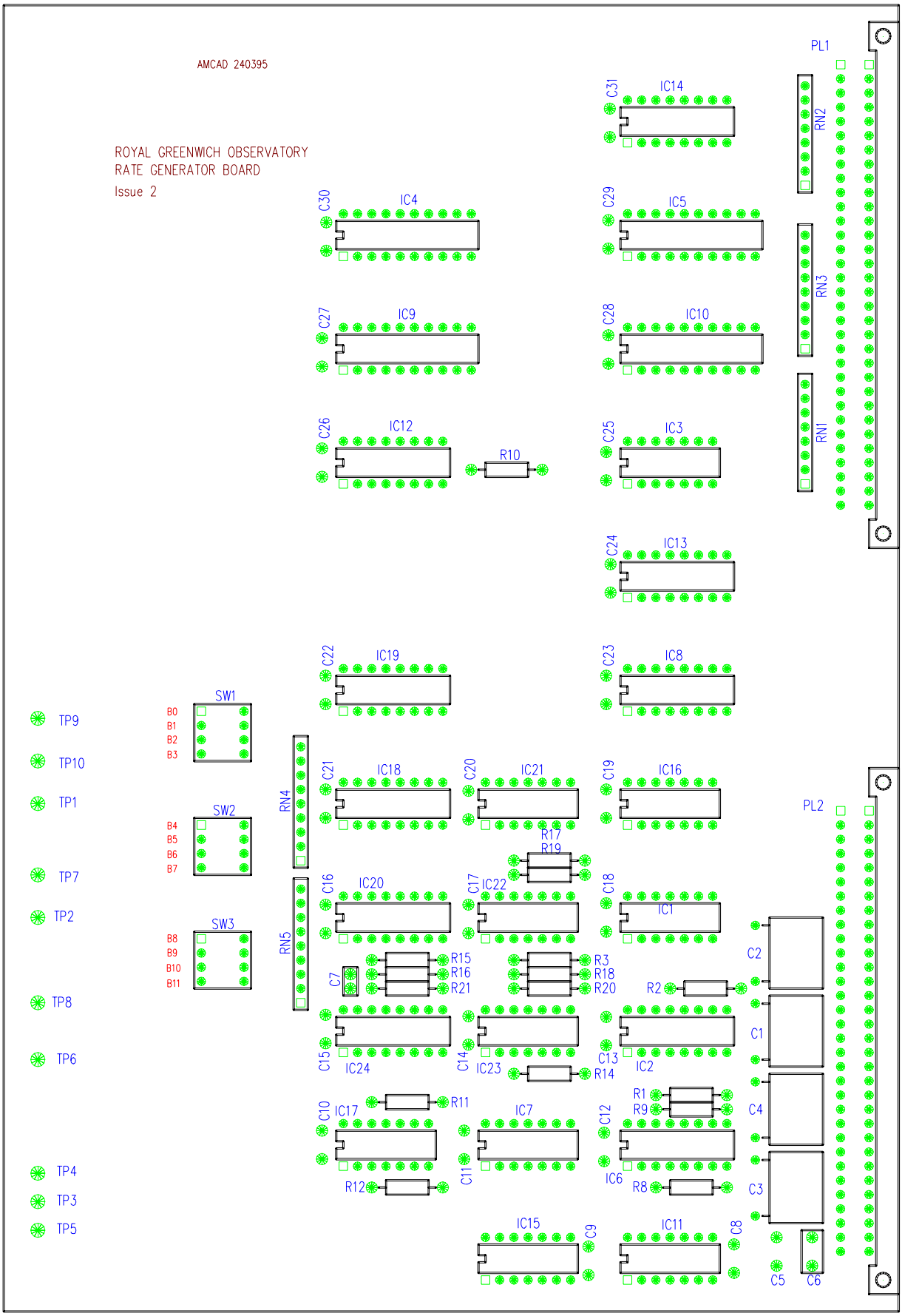
0100 1000 1011= $48B_{HEX}$ = 1163

$$f_{maxdem} = \frac{10^6}{(1163+1)} = 859.1 \text{ Hz or } 1.19 \text{ degs/sec } (@ 722.2 \text{ bits/deg})$$

In summary, the tabulated list of division ratios are.....

	Ratio(N+1)	Max rate (Hz)	max velocity(deg/s)
AZ tape encoder	2	500,000	1.15
EL/AZ	8	125,000	1.04
Cassegrain	801	1248.4	1.19
Prime/Nasmyth	1164	859.1	1.19

No explanation is given in the Marconi notes as to why the El/Az setting for max velocity is so near the 1deg limit, it's interesting to note that a division ratio of 7 would give the same velocity limit as the rotators i.e. 1.19deg/sec! but any change would need to be done in conjunction with the software scaling factor.



REDUCE TO 160mm

COMPONENT SIDE (LAYER 1)