# *WHT Marconi boards optimisation procedures*

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## Adjusting the Marconi Counter Boards (CTB)

## Introduction

The set-up and testing of this board is very well covered in Martin Fisher's May 1999 document "Testing the Marconi Servo Counter Board". That procedure was used successfully by Diego Cano in April 2005 but some anomalies where noticed particularly with respect to PCB link setting and corrections to manufacturing errors in the PCB tracks. These differences were discussed with Martin, and the procedure in this document is largely taken from the 1999 document but incorporating changes with changes using the correspondence between Diego and Martin.

## Circuit Description

The function of the Counter Board is to provide an analogue output representing the rate error of the particular drive on the telescope to which the board is assigned. The error voltage is passed to the APB board where it is integrated to produce the demand for the velocity loop. When the telescope is tracking normally the error voltage is very nearly zero.

The rate error is produced by an up-down 16-bit digital counter clocked by two serial pulse streams, one representing the demanded rate and the other the actual rate (incremental encoder output). The outputs of the counter are latched, when the counter is not changing, and the latch data buffered onto the input to a 16-bit DAC. The rate pulses and encoder pulses are received from the Rate Generator Board where they have been synchronised to different phases of the system clock as an anti-coincidence precaution. Either of these pulses will trigger a change in count, which will latch the counter value once it has had time to ripple through. There is also a 16-bit parallel data input directly to the DAC, allowing direct access. This enables the board to be used for direct velocity control of the Focus Drive. It also, fortuitously, allows the DAC linearity to be checked and the offset and span parameters to be adjusted. The DAC has a +/- 10V range with $0000_{hex}$ giving –10V out, $8000_{hex}$ giving 0V and FFFF giving +10V output.

There is provision on the board to select the direction of the rate inputs and also to limit the range of the counter to prevent overflow and thus wrap-around to zero.

## Tests and adjustments

The purpose of testing the counter board centres on checking the DAC performance particularly its linearity. Telescope tracking is the most critical phase of operation and at this time the counter is operating around zero counts. Note: a count is essentially an encoder bit (0.03 arc-seconds for the gear encoder or 0.008 arc-seconds for the tape encoder if it is connected instead of the gear encoder). It is important therefore that the DAC is reasonably linear around zero volts output.

The adjustments to carry out are to zero the output of the DAC for $8000_{hex}$ input (note this is zero counts with the sign bit set to produce mid range of the DAC) and to adjust the span to give +/-10V output for the two extremes of input. This adjustment is not critical because the counter always limits well before the maximum or minimum range.

The most important test to carry out is to ensure linearity of DAC output for a range of counts around zero, say +/- 16 counts. This can be extended in coarse jumps to the full DAC range. Other tests to perform are:
(a) to ensure bit-wise integrity of the DAC, i.e. to check that setting or clearing a bit on the DAC does not couple to other bits;
(b) to check that the counter limits properly and does not wrap to zero;
(c) check that counter latching operates properly and on receipt of both up and down encoder and rate pulses

## P**ROCEDURE**

### Outline

The only practicable method of testing the DAC is to write data directly to it. This is done using the auxiliary channel that is provided for direct control of velocity for some servomechanisms. The Focus Drive uses direct velocity control.

The CAMAC output registers (OR48) that write a data word to the rate generators are used to write to the auxiliary channel of the counter board, the Marconi crate back-plane being wired so that the inputs to the Rate Generator Board are also passed to the Counter Board. The 24-bit word is arranged so that the top 16 bits are data and the lower 8 bits are control.
**NB: I've noticed that this is not the case for the CASS and PRIME rotator counter board slots. Therefore for testing its best to use the FOCUS-, ALTITUDE- or AZIMUTH-Counter board position. The NASMYTH positions have not been tested yet, and I'm not sure if the back-plane has been wired appropriately. (RJP 20/02/2017)**

The utility CAMTEST which runs under the Engineer account on the DEC Alpha is used to write bit patterns to the appropriate CAMAC OR48 module. This has to be done with the TCS running, as the telescope must be in Computer Mode to obtain the necessary states on the Counter Board. However, if the TCS is running it is normally writing to all the CAMAC OR48s every twentieth of a second so any information written to a module is almost immediately over-written. There are two methods to avoid this:

(a) The second, unused, output register on the Focus Drive OR48 can be used, as this does not get over-written. In this case the cable linking the axis under investigation to its OR48 channel has to be switched to this unused channel.

(b) The CAMTEST program can take over the interrupt that normally triggers the 20Hz synchronous process in the TCS. In this case no cables need be switched.

Whichever method is used the testing technique is the same: a bit-pattern is written to the OR48 that sets up the Counter Board for directing the data portion of the pattern to the DAC. The resulting output voltage is monitored on a precision digital voltmeter connected to the output pins of the board (not directly to the DAC).

**System Preparation**

Not all the old Marconi boards had the buffer chips fitted and the link allowing CAMAC control of the data source enabled. It is therefore essential to make sure the board is chipped and configured for direct data control.

If the TCS is running it can remain running and does not have to be shut down. However it is always best to reboot the TCS after finishing to ensure that no CAMAC registers that are set up on start-up have been overwritten. If the CAMTEST 'disable interrupts' method is used then the TCS must be rebooted after finishing to re-establish the interrupts.

**Marconi system preparation:**

- **Ensure telescope is in ENGINEERING mode.**
- **Ensure that ALL power amplifier circuit breakers are switched OFF**
- **Shut down the Marconi crate power supplies (both the 5V and +/-15V)**
- **Ensure the CAMAC crate is switched off before inserting the connector into the unused focus drive OR48 module**

**Board preparation:**

- **Remove the Counter Board for the axis/drive under test from the Marconi crate.**
- **Make sure that IC23, IC24, IC28 and IC29 are fitted.**
- **For the old Marconi CTBs make sure that link 21 to 22 is made and 22 to 23 are unmade.**
- **For the new counter board, make sure link 9 is made.**
- **Ensure the hardware imposed speed limit is set to maximum (S1 all off, S2 all on)**
- **Put the board onto an extender board.**
- **For the old Marconi CTBs connect the DVM to connector PL1 pins 1c8 and 1c9 (the low lead to 1c9 because of the inversion in generating the differential signal from the DAC output.**
- **For the new counter board: connect the DVM to TP10 and TP9 (the low lead to TP10)**
- **Switch on Marconi crate power supplies.**

**CAMAC preparation:**

- **If using the unused channel of the Focus Drive OR48 then unplug the CAMAC cable from the OR48 channel of the drive that is under test and plug it in here. Otherwise leave cables alone.**

**TCS preparation:**

- **If TCS is not running, start it.**
- **Switch on the Oil pumps, to be able to switch to COMPUTER mode.**
- **Log into LPAS4 as 'engineer' with password 'ing_engineer'**
- **Start Camtest.**
- **Ensure that the power amps are OFF and then switch telescope to COMPUTER mode.**
- **If using the disable interrupt method then type this at the CAMTEST prompt: LAM 0 0 8 15 .This will stop the 20Hz interrupts from initiating the SYNC process and hence the lights will stop flashing on the CAMAC modules.**

- **If required, you can also stop the Dome motors from running all the time in COMPUTER mode by typing this at the CAMTEST prompt: EXEC 6 3 2 1 16 %X000000**

The Camtest utility can now be used to write to the counter board under test.

**Camtest procedure**

The camtest utility has a help function that provides basic operation information so type HELP and examine the topics provided.

To read from or write to a CAMAC location the command to use is described as:

EXECUTE B C N A F [ DATA [FUNCTION LABEL [ADDRESS LABEL]]]

The address and function labels can be used if desired but in this description we shall only use the data field.

The Marconi crate is on CAMAC branch 6 and is crate 1 so B = 6 and C = 1 but for the Nasmyth drives the crate would be 2. The station number, N, refers to the OR48 module of axis to be tested or if the unused channel of Focus Drive module is to be used. The data word is a combination of the control bits and data pattern to be sent.

The BCNAF allocations are as shown in the table below.

| **Axis/drive** | BCNAF (note F is normally 0 for a read and 16 for a write) | | | | |
|---|---|---|---|---|---|
| | B | C | N | A | F |
| ALTITUDE | 6 | 1 | 9 | 0 | 16 |
| AZIMUTH | 6 | 1 | 9 | 1 | 16 |
| FOCUS DRIVE | 6 | 1 | 11 | 0 | 16 |
| UNUSED CHANNEL | 6 | 1 | 11 | 1 | 16 |

**Data word bit allocation**

The format of the data word sent to the Rate Generator and Counter boards is shown in the following table. The bit pattern for normal tracking is shown as well as the minimum pattern for the test arrangement. For checking the counter limits the tracking bit pattern can be used.

| **Bit** | **Tracking** | **Test** | **Function** |
|---|---|---|---|
| 1 | 1 | 1 | TRACKING ON |
| 2 | 0 | 0 | SPARE |
| 3 | 1 | 1 | COMPUTER CONTROL ON |
| 4 | 1 | 0 | SERVO ON |
| 5 | 1 | 0 | CHANNEL SELECT (0 = auxiliary, 1 = counter) |
| 6 | 1 | 0 | COUNTER ENABLE |
| 7 | 1 or 0 | 0 | ENCODER SELECT ( =1 except for Cassegrain T/T) |
| 8 | 1 | 0 | RATE GENERATOR ENABLE |
| 9 | X | X | DATA BIT 1 (LSB) |
| 10 | X | X | 2 |
| 11 | X | X | 3 |
| 12 | X | X | 4 |
| 13 | X | X | 5 |
| 14 | X | X | 6 |
| 15 | X | X | 7 |
| 16 | X | X | 8 |
| 17 | X | X | 9 |
| 18 | X | X | 10 |
| 19 | X | X | 11 |
| 20 | X | X | 12 |
| 21 | X | X | 13 |
| 22 | X | X | 14 |
| 23 | X | X | 15 |
| 24 | X | X | SIGN BIT |

Example: EXECUTE 6 1 11 1 16 %X800005

will write $8000_{hex}$ to the unused channel of the Focus Drive module and should produce exactly 0V from the DAC. Note that the VMS symbol for a hex string, %X, must precede the data if it is to be in HEX.

Offset and Span adjustment

The Span and offset adjustments are called gain (VR2) and range (VR1) on the circuit diagram. The gain control determines the minimum to maximum voltage span, nominally 20V, and the range control moves this span around zero. The controls are interactive and, because of non-linearity in the DAC, it may not be possible to achieve –10V, 0V and +10V exactly. A reasonable compromise should be sought but note that the zero condition is far more important than the span accuracy.
Perform the following measurements, using a copy of the Counter Test Sheet appended to this document to note down the results.

- **Write $000005_{hex}$ to the counter and note the DAC output on the DVM**
- **Write $800005_{hex}$ to the counter and note the DAC output on the DVM**
- **Write $FFFF05_{hex}$ to the counter and note the DAC output on the DVM**
- **Adjust the span control to get close to +/-9.4V maximum and minimum output.**
- **Adjust the zero control to get 0V output at mid-range ($8000_{hex}$)**
- **Repeat as necessary to get optimum result but with an accurate zero.**
- **Calculate the average bit value and write this on the test sheet: (total span voltage divided by $2^{16}$ or 65536).**

**Linearity test**

This test is in two parts. First, the linearity close to zero is tested. This is done by stepping through 33 bits, centred about zero, in one-bit increments. This is the important range of the DAC from the point of view of normal tracking. If tracking problems persist but this range of values is OK it may be necessary to test a wider range. Second, the whole range of the DAC is tested at 33 evenly spaced points. A table of test codes (i.e. the data part of the word written to the OR48) is included on the Counter Test Sheet appended to this document. This table also shows the expected DAC output voltage, assuming a +/-10V linear span and exact zero point. An adjacent column is provided for writing in the expected DAC output given the bit value calculated above and another column is provided for recording the actual output measured by the DVM. The important quality of the DAC is that it is monotonic and reasonably linear around the zero point. Variations in the bit value of 25% or so can be tolerated in this application. Missing codes or abnormally large bit values will lead to poorer tracking as the servo error switches through these codes trying to achieve the correct DAC output which will maintain the required voltage at the output of the integrator on the process board.

**Bit-wise integrity**

This is a standard digital systems test, the aim of which is to detect any bit-interdependency in the circuit or in the DAC. To detect errors in the low order bits due to a high order bit being set requires careful evaluation of the results and if necessary an bit-increment test may be required around any suspect point in the range. Problems with high order bits affecting low order bits may cause peculiar behaviour during slew acceleration and deceleration but otherwise not upset tracking performance because the value in the counter is generally larger during these phases. If, however, a low order bit change causes a higher order bit change then serious tracking problems may be experienced. The test requires two codes to be written: $5555_{hex}$ and $AAAA_{hex}$, which are, of course, alternate bits. The results can be entered on the Counter Test Sheet.

**Counter limits**

To test the counter limits the counter must receive pulses from one source and the easiest provider is the Rate Generator itself. The technique used will depend on whether the Camtest programme is blocking the synchronous process interrupts. If this is the case then a word can be written to the rate generator with the appropriate code for normal tracking. This will allow rate pulses through to the counter, which will quickly fill up because if there are no corresponding encoder pulses supplied when the telescope is stationary. The value in the counter should then be limited by the code set on switches S1 and S2 and a constant voltage will result from the DAC. If this is not the case and the DAC output is unsteady, the counter may be wrapping around at zero due to some fault in the logic. The other limit can be tested by changing the sign bit of the code written to the rate generator. The results can be entered on the Counter Test Sheet.

# *CTB Record Sheet*

Module: Test Date: Tested by:

*SPAN AND OFFSET ADJUSTMENT*

| Code (hex) | Initial O/P | Adjust Span | Adjust Zero |
|---|---|---|---|
| 0 | | | |
| 8000 | | | |
| FFFF | | | |

*COUNTER TEST TABLE OF CODES*

| Zero zone linearity | | | Full scale linearity | | |
|---|---|---|---|---|---|
| Code (hex) | Expected O/P (mV) | Measured O/P (mV) TP9 to TP10 | Code (hex) | Expected O/P (V) | Measured O/P (V) TP9 to TP10 |
| 7FF0 | -4.590 | | 0 | -9.400 | |
| 7FF1 | -4.303 | | 800 | -8.812 | |
| 7FF2 | -4.016 | | 1000 | -8.225 | |
| 7FF3 | -3.729 | | 1800 | -7.637 | |
| 7FF4 | -3.442 | | 2000 | -7.050 | |
| 7FF5 | -3.156 | | 2800 | -6.462 | |
| 7FF6 | -2.869 | | 3000 | -5.875 | |
| 7FF7 | -2.582 | | 3800 | -5.287 | |
| 7FF8 | -2.295 | | 4000 | -4.700 | |
| 7FF9 | -2.008 | | 4800 | -4.112 | |
| 7FFA | -1.721 | | 5000 | -3.525 | |
| 7FFB | -1.434 | | 5800 | -2.937 | |
| 7FFC | -1.147 | | 6000 | -2.350 | |
| 7FFD | -0.861 | | 6800 | -1.762 | |
| 7FFE | -0.574 | | 7000 | -1.175 | |
| 7FFF | -0.287 | | 7800 | -0.587 | |
| 8000 | 0.000 | | 8000 | 0.000 | |
| 8001 | 0.287 | | 8800 | 0.588 | |
| 8002 | 0.574 | | 9000 | 1.175 | |
| 8003 | 0.861 | | 9800 | 1.763 | |
| 8004 | 1.147 | | A000 | 2.350 | |
| 8005 | 1.434 | | A800 | 2.938 | |
| 8006 | 1.721 | | B000 | 3.525 | |
| 8007 | 2.008 | | B800 | 4.113 | |
| 8008 | 2.295 | | C000 | 4.700 | |
| 8009 | 2.582 | | C800 | 5.288 | |
| 800A | 2.869 | | D000 | 5.875 | |
| 800B | 3.156 | | D800 | 6.463 | |
| 800C | 3.442 | | E000 | 7.050 | |
| 800D | 3.729 | | E800 | 7.638 | |
| 800E | 4.016 | | F000 | 8.225 | |
| 800F | 4.303 | | F800 | 8.813 | |
| 8010 | 4.590 | | FFFF | 9.400 | |

*Bit-wise integrity*

| Code (hex) | Expected O/P (mV) | TP9 to TP10 O/P (V) |
|---|---|---|
| 5555 | -3.133 | |
| AAAA | 3.133 | |

*Counter Limits*

| S1 Setting | Expected O/P (V) | TP9 to TP10 O/P (V) | S2 Setting | Expected O/P (V) | TP9 to TP10 O/P (V) |
|---|---|---|---|---|---|
| 0 0 0 0 | -7.144 | | 0 0 0 0 | 9.4 | |
| 0 0 0 1 | -7.285 | | 0 0 0 1 | 9.259 | |
| 0 0 1 0 | -7.426 | | 0 0 1 0 | 9.118 | |
| 0 0 1 1 | -7.567 | | 0 0 1 1 | 8.977 | |
| 0 1 0 0 | -7.708 | | 0 1 0 0 | 8.836 | |
| 0 1 0 1 | -7.849 | | 0 1 0 1 | 8.695 | |
| 0 1 1 0 | -7.99 | | 0 1 1 0 | 8.554 | |
| 0 1 1 1 | -8.131 | | 0 1 1 1 | 8.413 | |
| 1 0 0 0 | -8.272 | | 1 0 0 0 | 8.272 | |
| 1 0 0 1 | -8.413 | | 1 0 0 1 | 8.131 | |
| 1 0 1 0 | -8.554 | | 1 0 1 0 | 7.99 | |
| 1 0 1 0 | -8.695 | | 1 0 1 0 | 7.849 | |
| 1 0 1 1 | -8.836 | | 1 0 1 1 | 7.708 | |
| 1 1 0 0 | -8.977 | | 1 1 0 0 | 7.567 | |
| 1 1 0 1 | -9.118 | | 1 1 0 1 | 7.426 | |
| 1 1 1 0 | -9.259 | | 1 1 1 0 | 7.285 | |
| 1 1 1 1 | -9.4 | | 1 1 1 1 | 7.144 | |