

Testing the Marconi Servo Counter Board

Martin Fisher 23 May 1999-05-23

Introduction

Circuit Description

The function of the Counter Board is to provide an analogue output representing the rate error of the particular drive of the telescope to which the board is assigned. This error voltage is passed to the Analogue Process Board where it is integrated to produce the demand for the velocity loop. When the telescope is tracking well the error voltage is zero or very nearly zero.

The rate error is produced by an up-down 16-bit digital counter that is clocked by two serial pulse streams, one representing the demanded rate and one representing the actual rate (from the incremental encoder). The outputs of the counter are latched, at a time when the counter is not changing, and the latch outputs buffered onto an input bus to a 16-bit DAC. The rate pulses and encoder pulses are received from the Rate Generator Board where they have been synchronised to different phases of the system clock as an anti-coincidence precaution. Either of these pulses will trigger a signal which will latch the counter value after it has had time to ripple through. There is also a 16-bit parallel data input to this bus, allowing direct access to the DAC. This enables the board to be used in a different mode, e.g. for direct velocity control of the Focus Drive. It also, fortuitously, allows the DAC linearity to be checked and the offset and span parameters to be adjusted. The DAC has a +/- 10V range with 0000_{hex} giving -10V out, 8000_{hex} giving 0V and FFFF giving +10V output.

There is provision on the board to select the direction of the rate inputs and also to limit the range of the counter to prevent overflow and thus wrap-around to zero.

Tests and adjustments

The purpose of testing the counter board centres on the DAC performance. Telescope tracking is the most critical phase of operation and at this time the counter is operating around zero counts. Note: a count is essentially an encoder bit (0.03 arc-seconds for the gear encoder or 0.008 arc-seconds for the tape encoder if it is connected instead of the gear encoder). It is important therefore that the DAC is reasonably linear around zero volts output.

The adjustments to carry out are to zero the output of the DAC for 8000_{hex} input (note this is zero counts with the sign bit set to produce mid range of the DAC) and to adjust the span to give +/-10V output for the two extremes of input. This adjustment is not critical because the counter always limits well before the maximum or minimum range.

The most important test to carry out is to ensure linearity of DAC output for a range of counts around zero, say +/- 16 counts. This can be extended in coarse jumps to the full DAC range. Other tests to perform are:

- (a) to ensure bit-wise integrity of the DAC, i.e. to check that setting or clearing a bit on the DAC does not couple to other bits;
- (b) to check that the counter limits properly and does not wrap to zero;
- (c) that counter latching operates properly and on receipt of both up and down encoder and rate pulses

PROCEDURE

Outline

The only practicable method of testing the DAC is to write data directly to it. This is done using the auxiliary channel that is provided for direct control of velocity for some servomechanisms. The Focus Drive uses direct velocity control and so do the experimental type 2B servo cards.

The CAMAC output registers (OR48) that write a data word to the rate generators are used to write to the auxiliary channel of the counter board, the Marconi crate back-plane being wired so that the inputs to the Rate Generator Board are also passed to the Counter Board. The 24-bit word is arranged so that the top 16 bits are data and the lower 8 bits are control.

The utility CAMTEST which runs under the Engineer account on the DEC Alpha is used to write bit patterns to the appropriate CAMAC OR48 module. This has to be done with the TCS running as the telescope must be in Computer Mode to obtain the necessary states on the Counter Board. However, if the TCS is running it is

normally writing to all the CAMAC OR48s every twentieth of a second so any information written to a module is almost immediately over-written. There are two methods to avoid this:

- (a) The second, unused, output register on the Focus Drive OR48 can be used as this does not get over-written. In this case the cable linking the axis under investigation to its OR48 channel has to be switched to this unused channel.
- (b) The CAMTEST program can take over the interrupt that normally triggers the 20Hz synchronous process in the TCS. In this case no cables need be switched.

Whichever method is used the testing technique is the same: a bit-pattern is written to the OR48 which sets up the Counter Board for directing the data portion of the pattern to the DAC. The resulting output voltage is monitored on a precision digital voltmeter connected to the output pins of the board (not directly to the DAC).

System Preparation:

Not all the old Marconi boards had the buffer chips fitted and the link allowing CAMAC control of the data source enabled. The first thing to do then is to make sure the board is chipped and linked for direct data control.

If the TCS is running it can remain running and does not have to be shut down. However it is always best to reboot the TCS after finishing to ensure that no CAMAC registers that are set up on start-up have been overwritten. If the CAMTEST 'disable interrupts' method is used then the TCS must be rebooted after finishing to re-establish the interrupts.

Marconi system preparation:

- ***Ensure telescope is in ENGINEERING mode.***
- ***Ensure that ALL power amplifier circuit breakers are switched OFF***
- ***Shut down the Marconi crate power supplies (both the 5V and +/-15V).***

Board preparation:

- ***Remove the Counter Board for the axis/drive under test from the Marconi crate.***
- ***Make sure that IC23, IC24, IC28 and IC29 are fitted.***
- ***For the old Marconi counter: make sure that link 21 to 22 is made and 22 to 23 is unmade.***
- ***For the new counter board: ensure that link 3 is in position 2-3***
- ***Put the board onto an extender board.***
- ***For the old Marconi counter: connect the DVM to connector PL1 pins 1c8 and 1c9 (the low lead to 1c9 because of the inversion in generating the differential signal from the DAC output.***
- ***For the new counter board: connect the DVM to TP10 and TP9 (the low lead to TP10)***
- ***Switch on Marconi crate power supplies.***

CAMAC preparation:

- ***If using the unused channel of the Focus Drive OR48 then unplug the CAMAC cable from the OR48 channel of the drive that is under test and plug it in here. Otherwise leave cables alone.***

TCS preparation:

- ***If TCS is not running, start it.***
- ***Log into LPAS4 as 'engineer' with password ***** (see CAMAC manual)***
- ***Start Camtest.***
- ***Ensure that the power amps are OFF and then switch telescope to COMPUTER mode.***
- ***If using the disable interrupt method then type this at the CAMTEST prompt:***

LAM 0 0 8 15

This will stop the 20Hz interrupts from initiating the SYNC process and hence the lights will stop flashing on the CAMAC modules.

The Camtest utility can now be used to write to the counter board under test.

Camtest procedure

The camtest utility has a help function which provides basic operation information so type HELP and examine the topics provided. To read from or write to a CAMAC location the command to use is described as:

EXECUTE B C N A F [DATA [FUNCTION LABEL [ADDRESS LABEL]]]

The address and function labels can be used if desired but in this description we shall only use the data field.

The Marconi crate is on CAMAC branch 6 and is crate 1 so B = 6 and C = 1 but for the Nasmyth drives the crate would be 3. The station number, N, depends on the OR48 module of axis to be tested or is the Focus Drive module if the unused channel approach is to be used. The data word is a combination of the control bits and data pattern to be sent.

Table of BCNAF allocations

The BCNAF allocations are as shown in the table below.

Axis/drive	BCNAF (note F is normally 0 for a read and 16 for a write)				
	B	C	N	A	F
ALTITUDE	6	1	9	0	16
AZIMUTH	6	1	9	1	16
CASSEGRAIN TURNTABLE	6	1	10	0	16
PRIME FOCUS TURNTABLE	6	1	10	1	16
FOCUS DRIVE	6	1	11	0	16
UNUSED CHANNEL	6	1	11	1	16
NASMYTH GHRIL T/T	6	2			16
NASMYTH UES T/T	6	2			16

Data word bit allocation

The format of the data word sent to the Rate Generator and Counter boards is shown in the following table. The bit pattern for normal tracking is shown as well as the minimum pattern for the test arrangement. For checking the counter limits the tracking bit pattern can be used.

Bit	Tracking	Test	Function
1	1	1	TRACKING ON
2	0	0	SPARE
3	1	1	COMPUTER CONTROL ON
4	1	0	SERVO ON
5	1	0	CHANNEL SELECT (0 = auxiliary, 1 = counter)
6	1	0	COUNTER ENABLE
7	1 or 0	0	ENCODER SELECT (=1 except for Cassegrain T/T)
8	1	0	RATE GENERATOR ENABLE
9	X	X	DATA BIT 1 (LSB)
10	X	X	2
11	X	X	3
12	X	X	4
13	X	X	5
14	X	X	6
15	X	X	7
16	X	X	8
17	X	X	9
18	X	X	10
19	X	X	11
20	X	X	12
21	X	X	13
22	X	X	14
23	X	X	15
24	X	X	SIGN BIT

Example: EXECUTE 6 1 11 1 16 %X800005

will write 8000_{hex} to the unused channel of the Focus Drive module and should produce exactly 0V from the DAC. Note that the VMS symbol for a hex string, %X, must precede the data if it is to be in HEX.

Offset and Span adjustment

The Span and offset adjustments are called gain (VR2) and range (VR1) on the circuit diagram. The gain control determines the minimum to maximum voltage span, nominally 20V, and the range control moves this span around zero. The controls are interactive and, because of non-linearity in the DAC, it may not be possible to achieve -10V, 0V and +10V exactly. A reasonable compromise should be sought but note that the zero condition is far more important than the span accuracy.

Perform the following measurements, using a copy of the Counter Test Sheet appended to this document to note down the results.

- Write 000005_{hex} to the counter and note the DAC output on the DVM
- Write 800005_{hex} to the counter and note the DAC output on the DVM
- Write FFFF05_{hex} to the counter and note the DAC output on the DVM
- Adjust the span control to get close to +/-10V maximum and minimum output.
- Adjust the zero control to get 0V output at mid-range (8000_{hex})
- Repeat as necessary to get optimum result but with an accurate zero.
- Calculate the average bit value and write this on the test sheet: (total span voltage divided by 2¹⁶ or 65536).

Linearity test

This test is in two parts. First, the linearity close to zero is tested. This is done by stepping through 33 bits, centred about zero, in one-bit increments. This is the important range of the DAC from the point of view of normal tracking. If tracking problems persist but this range of values is OK it may be necessary to test a wider range. Second, the whole range of the DAC is tested at 33 evenly spaced points.

A table of test codes (i.e. the data part of the word written to the OR48) is included on the Counter Test Sheet appended to this document. This table also shows the expected DAC output voltage, assuming a +/-10V linear span and exact zero point. An adjacent column is provided for writing in the expected DAC output given the bit value calculated above and another column is provided for recording the actual output measured by the DVM.

The important quality of the DAC is that it is monotonic and reasonably linear around the zero point. Variations in the bit value of 25% or so can be tolerated in this application. Missing codes or abnormally large bit values will lead to poorer tracking as the servo error switches through these codes trying to achieve the correct DAC output which will maintain the required voltage at the output of the integrator on the process board.

Bit-wise integrity

This is a standard digital systems test, the aim of which is to detect any bit-interdependency in the circuit or in the DAC. To detect errors in the low order bits due to a high order bit being set requires careful evaluation of the results and if necessary an bit-increment test may be required around any suspect point in the range. Problems with high order bits affecting low order bits may cause peculiar behaviour during slew acceleration and deceleration but otherwise not upset tracking performance because the value in the counter is generally larger during these phases. If, however, a low order bit change causes a higher order bit change then serious tracking problems may be experienced.

The test requires two codes to be written: 5555_{hex} and AAAA_{hex} which are, of course, alternate bits. The results can be entered on the Counter Test Sheet.

Counter limits

To test the counter limits the counter must receive pulses from one source and the easiest provider is the Rate Generator itself. The technique used will depend on whether the Camtest programme is blocking the synchronous process interrupts. If this is the case then a word can be written to the rate generator with the appropriate code for normal tracking. This will allow rate pulses though to the counter, which will quickly fill up because there are no corresponding encoder pulses being fed back as the telescope is static. The value in the counter should then be the limited according to the code set and a constant voltage should result from the DAC. If this is not the case and the DAC is wavering then the counter may be wrapping around to zero due to some fault in the logic. The other limit can be tested by changing the sign bit of the code written to the rate generator. The results can be entered on the Counter Test Sheet.

COUNTER TEST SHEET

Counter Module:..... Test Date:..... Tested by:.....

SPAN AND OFFSET ADJUSTMENT

Code (hex)	Initial O/P	Adjust Span	Adjust zero	Adjust Span	Adjust zero
0000					
8000					
FFFF					

AVERAGE BIT VALUE

Average bit value = total span/65536 and is nominally 20V/65536 = 0.000305V or 0.3mV per bit

Actual average bit value: $(\text{max-span} - \text{min-span}) = \frac{\quad + \quad}{65536} = \frac{\quad}{65536} = \quad \text{mV/bit}$

COUNTER TEST TABLE OF CODES

Zero zone linearity			Full scale linearity		
Code (hex)	Expected O/P (mV)	DAC O/P mV	Code (hex)	Expected O/P (V)	DAC O/P V
7FF0	-4.883		0000	-10	
7FF1	-4.578		0800	-9.375	
7FF2	-4.272		1000	-8.750	
7FF3	-3.967		1800	-8.125	
7FF4	-3.662		2000	-7.500	
7FF5	-3.357		2800	-6.875	
7FF6	-3.052		3000	-6.250	
7FF7	-2.747		3800	-5.625	
7FF8	-2.441		4000	-5.000	
7FF9	-2.136		4800	-4.375	
7FFA	-1.831		5000	-3.750	
7FFB	-1.526		5800	-3.125	
7FFC	-1.221		6000	-2.500	
7FFD	-0.916		6800	-1.875	
7FFE	-0.610		7000	-1.25	
7FFF	-0.305		7800	-0.625	
8000	0.0		8000	0.0	
8001	0.305		8800	0.625	
8002	0.610		9000	1.250	
8003	0.916		9800	1.875	
8004	1.221		A000	2.500	
8005	1.526		A800	3.125	
8006	1.831		B000	3.750	
8007	2.136		B800	4.375	
8008	2.441		C000	5.000	
8009	2.747		C800	5.625	
800A	3.052		D000	6.250	
800B	3.357		D800	6.875	
800C	3.662		E000	7.500	
800D	3.967		E800	8.125	
800E	4.272		F000	8.750	
800F	4.578		F800	9.375	
8010	4.883		FFFF	10.000	

Bit-wise integrity

Code (hex)	Expected O/P	DAC O/P V	Code (hex)	Expected O/P	DAC O/P V
5555	-3.333		AAAA	3.333	

Counter limits

+ve limit	Expected O/P	DAC O/P V	-ve limit	Expected O/P	DAC O/P V