Proposal for improving the performance of The NAOMI Wave Front Sensor.

Peter Moore - April 2001.

Introduction.

This report intends to address the current deficiencies of the NAOMI Wave Front Sensor performance and provide workable options that can be employed to overcome them. The document is structured in the following way: After a summary of conclusions reached by this document, a brief enumerated list of problems is presented followed by a discussion of each item. This is followed by a list of possible options available to overcome specific problems and a conclusion that outlines the order of preference for action to be taken. At the end of this report are the workings of an analysis performed to reach one of the conclusions, and a list of references used in this document.

Summary of Conclusions.

1. Continue to look for funds to construct a laser guide star or, failing this, study the possibility of modifying the wave front sensor to allow adaptive sub-aperture selection.
2. Investigate optical means of improving the through-put efficiency to the wave front sensor.
3. Conduct a search for improved red response detectors for use when NAOMI supplies a science focus at visible wavelengths.
4. Invest in the development of MARCONI L3 detector technology for possible returns in a time frame of two - three years. Meanwhile investigate the potential of alternate noise free techniques.
5. Improve the bandwidth (i.e frame rate) of the system without resorting to a twin detector configuration. Acomplish this by modifications to the current hardware.

Statement of actual limitations on current performance.

1. Problem 1 - **Photon starvation**.
   a.) Guide star source magnitude.
   b.) Optical transmission of system.
   c.) Detector conversion efficiency - especially for visible science focus.
   d.) Low signal to noise ratio of detector system in majority of observations.

2. Problem 2 - **Low bandwidth**.
   a.) The current controller cannot supply the required frame rate to support the correction bandwidth required by NAOMI.

Available options to improve performance.

1a. Find / generate brighter guide star

a.) Laser guide star
b.) Reduce number of sub-apertures
c.) Increase available spectral bandwidth to the WFS.

Problem 1a. - Discussion.

Given any option available, the implementation of a laser guide star system would be enabling to the full possibilities of NAOMI and resolve problem 1

entirely. Given that this option is not feasible in the near future, the possibility of reducing the number of sub-apertures across the primary mirror surface would increase the flux available for wave front sensing. This would reduce the effectiveness of the correction by some factor that would seem to correspond to the seeing conditions at any one time and hence potentially provide better corrected images with faint guide stars under some conditions. However, with the current Shack-Hartman WFS, this would need to be implemented primarily in the optical path and be cumbersome to install and operate. This would have the added complication of developing software to interpolate between the 'quantized' sub-apertures and driving the DM elements. Another approach that would allow a variable number of sub-apertures to be selected as conditions determined is possible by changing the WFS methodology to a curvature type WFS design. This approach would allow sub-aperture selection to be done in software without restriction of the optical configuration.

Conclusion 1a.

The best option is obviously to keep looking for a way to implement the laser guide star system. Alternatively a feasibility study of changing to a curvature type sensor should be undertaken to facilitate adaptive sub-aperture selection dependent on observing conditions.

1b. Improve optical transmission efficiency

a.) Reduce number of optical surfaces

b.) Improve anti-reflection coatings

Problem 1b. - Discussion.

Both of these stated options (and any that I haven't thought of !) are outside the domain of my expertise. I therefore suggest that someone with the required skills investigate a method of improving the optical efficiency.

Conclusion 1b.

That a study be undertaken to look at improvements in the optical efficiency of the NAOMI WFS beam path.

1c. Improve detector conversion efficiency.

a.) Improve antireflection coating

b.) Improve detector quantum efficiency in selected wavelengths.

Problem 1c. - Discussion.

Considering that the current WFS detectors have comparatively excellent quantum efficiency, gains from selective coatings (using for example Lumigen for extended blue response) would be restricted to approximately 7% improvement if 'blue' reference stars are selected. However, when optical instruments are fed from the NAOMI focus it would be very advantageous to improve the WFS detectors red response. This could be most easily achieved by replacement of the detector itself by a thick and red optimised device.

Conclusion 1c.

Enquiries should be made to MARCONI (and others) to find suitable red optimised detector availability.

1d. Reduce signal noise component - improve s/n ratio.

a.) Improve detector and/or controller characteristics.

Problem 1d. - Discussion.

Fundamental to the success of photon detection is the optimisation of signal to noise ratio. Given that the WFS is starved of photons in the majority of occasions the problem reduces to one of reducing (or eliminating) electronic noise in the signal. MARCONI is now developing a detector with a built-in gain stage that amplifies the collected electrons to a level above the electronic noise floor at the detector output. These detectors (called L3 devices) can photon count if the incidence of photons is sufficiently low so that no more than one photon per pixel is collected in each pixel before reading out. If photon pileup does occur, the output is still available but with much degraded linearity. There are three modes of operation that can be employed with these detectors. These are listed below with the effect on signal to noise ratio that occurs.

1. Photon counting - Increase in SNR. Only usable in very low light conditions.
2. Non linear mode - Apparent SNR degradation due to photon pileup.
3. Normal mode - Same SNR as current detector.

It is seen that in photon counting mode and at illumination levels that are below approximately 3 photons per frame readout (using a QE of 35%), an improvement of two for SNR can be made when the SNR is equal to 1. In any conditions with increased illumination, no improvement to the performance is possible. What is needed is an elimination of the noise component for all conditions. The use of these detectors for wave front sensing requires that the conditions required by NAOMI be met. Currently the conditions listed below are still outstanding however, improvements in this family are promised for this year. A reasonable estimate for when all conditions can be met is two years.

1. Availability of suitable format.
2. Equivalent quantum efficiencies to CCD39 (currently at 35% peak).
3. Frame rates that can be achieved to satisfy NAOMI specifications.

An alternative to an investment in a new detector technology is outlined in this document in section 2, Option 3 and refers to a technique of sampling the signal + noise across a wide bandwidth. These data are then decimated in the frequency regime to limit the overall detection bandwidth to that of the detector signal and eliminate the out of band noise. This alternative would use the existing detectors and remove the dominant noise components from the signal at all flux levels and modes of use.

Conclusion 1d.

That a current technology MARCONI L3 detector be acquired for investigation purposes. The application of this device to an acquisition and finder camera could well be used as a test bed for the technology and allow deductions to be made with respect to its application to wave front sensing. In parallel, that the alternate technique for elimination of dominant noise sources be fully investigated.

2. Remove hardware limitation on frame rate

a.) Improve detector / controller hardware.

b.) Implement a two detector parallel system.

Problem 2 - Discussion.

In order to identify the limiting elements that prevent a one detector / SDSU system from delivering the required frame rate, a critical analysis of timing was undertaken. The result of this analysis is presented in appendix A. In conclusion, this analysis suggests that there are two "bottle necks" that prevents the required bandwidth from being achieved with the current hardware. These are:

a.) Lack of a First In First Out buffer (FIFO) to de-couple the burst pixel rate of the windowed readout mode from the continuous maximum pixel rate supported by the data down link.

b.) Video processing hardware that limits the conversion speed to the maximum rate of the Analog to Digital converter (ADC). This is currently a 1Mpix / channel pixel rate.

Several options to increase the frame rate are now presented and warrant further investigation:

Option 1. Modification to existing SDSU hardware.

A program of modifications could be implemented to the current hardware to remove the above mentioned limitations and increase the frame rate to that required i.e. 1000Hz. Two factors make this approach feasible with relatively low risk. These factors are:

a). The data current data pipeline that includes the delivery of image data to the array of C40 DSP's restricts the data word length to 14 bits. Currently the ADCs' are 16 bit 1 megasample devices which provide for a maximum of 32,000 e- dynamic range from the ccd's at approximately 0.5e- / adu. However, the truncation of the data path to 14 bits means that only 8,000e- can be accumulated before digital saturation takes place. Assuming that 8,000 e- dynamic range is sufficient for the application, a fast 14 bit ADC could be substituted which would give the required reduction in pixel processing time. Modern fast 14 bit ADCs' can sample at up to 10 Megasamples / second.

b). If the argument above is allowed, then suitable ADC devices exist that incorporate a FIFO element within the device. One such converter is the Texas Instrument THS14F03; A 3 megasample per second device with a 32 level FIFO incorporated on the silicon. This device would give a frame rate (based on the analysis presented in Appendix A) of 769 frames / second worst case and 1010 frames / second best case for a 6 x 6 sub-aperture x 72 readout scheme).

Before implementing such a scheme a more detailed analysis needs to be performed on the existing SDSU Video Processor boards to assure that the analog processing electronics could handle the increase in pixel rate. The increase is a factor of three so the possibility of the existing electronics handling the load is relatively high, therefore warranting the effort of analysis.

This approach, if feasible, would lead to an increase in readout noise (possibly of order 14 e- rms.).

Option 2. Implementation of a dual CCD system.
Implementing a dual detector system with beam splitter to increase frame rate actually exacerbates problem 1, that of photon starvation, by reducing the number of photons for each detector by less than half (at least 2% additional photon loss). In addition the signal to noise ratio degrades considerably to that currently obtained because both detectors contribute noise while the signal is to each detector is halved i.e. double the noise and half the signal. The implementation however, would not entail any modifications to existing hardware. Signal to noise ratio would decrease (i.e. become worse) by a factor of approximately 2.

Option 3. Purpose build specific noise cancelling high speed video boards.
The separate paper titled 'Noise Free Detectors - Including Wave Front Sensors' presents a novel approach (in astronomy) to achieving high speed readout of a CCD whilst preserving or possibly reducing the current noise contribution of the detector. In a similar manner to option 1, a high speed Video Processor would be built to achieve the required frame rate and pre-process the pixel data to remove the white and 1/f spectral noise of the readout electronics. This approach requires that a complete video signal processing chain be designed, optimised and built. This electronics would be incorporated on a circuit card compatible with the current SDSU controllers. An additional benefit of this option is the possibility of including a new and specific purpose data down link that removes the current limitation of the controller data down link bandwidth and would interface directly with the DSP array of the WFS. In this way the maximum frame rate of the system would be limited by the CCD detector itself and not by the controller. With the inclusion of purpose designed processing algorithms (ideally run in an upgraded DSP array) it is expected that noise cancellation at the required frame rates would be complete - thus producing noise free data.

Option 4. Make the system more parallel.
If the limiting element to achieving the frame rate is the serial manner that pixels are processed, An almost linear increase of performance can be achieved by making the system more parallel. To this end, if we could process eight channels of pixels in parallel within the current hardware architecture, then a frame rate of 1000 Hz would be achievable. The current CCD used in the WFS is a CCD39 - 01 with four video outputs available. This limits the degree of parallelism to 4 channels. An alternative detector is the (relatively) new CCD50 available from MARCONI. This device has the same pixel size and a split format of 128 x 68 x 2 giving a total of 17408 pixels in two segments. This detector has been specifically designed for high frame rate applications and provides 16 channels of video output. Thus, with one half of this device, assuming that the 68 pixels in one dimension give enough coverage, eight channels could be processed in parallel to give (almost) double the currently available frame rate i.e. 1200 Hz. To accomplish this the CCD would need to be purchased and fitted, the current SDSU upgraded to provide eight channels of video processing (2 more Video Boards) and, of

equal importance, hardware modifications to allow the insertion of a FIFO in the controller data path.

Problem 2. Conclusions

Considering the options available (i.e. improve controller hardware, upgrade the CCD, or use a dual system), it is apparent that the dual detector solution to the frame rate problem (Option 2) is the least attractive for the following reasons.

a.) This solution will physically reduce any available signal and introduces extra noise that will cause an overall degradation of WFS performance.
b.) This solution leads to increased system complexity with resulting problems of maintenance, optical alignment, and control software.

The upgrade of the WFS to another CCD (Option 4) would provide the performance with comparable noise and QE performance as currently achieved but at the expense of much detailed design engineering in many disciplines (Optical, Mechanical, and Electronic). This upgrade path would only be feasible if the loss of 12 pixels from one dimension of the CCD is acceptable. The detector is actually 128 x 136 pixels in format. If this size increase could be gainfully used, then the extra region could be controlled from the second SDSU controller to provide the same (1000 Hz +) frame rate with the larger format.

Option 1 provides the quickest and least risk opportunity to achieve the desired frame rate. This would however, depend on the favourable outcome of a more exhaustive analysis of the SDSU Video board performance under the increased pixel rate, the acceptance of the reduced dynamic range, and possibly increased noise figure. Under these conditions a plug in piggyback board that occupies the space of the current ADC could be built to accommodate the modification.

Option 3 carries more risk than option 1 but would potentially provide the added benefit of reduced readout noise. The design process would be limited to just one discipline; Electronics. This option also enables the free selection of an alternate data down link architecture to be compatible with proposed upgrades to the WFS DSP array.

In summary I would recommend that option 1 be further explored. If found not to be feasible, option 3 to be implemented.

References.

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6. CCD50 - Issue 1, Marconi Applied Technology, September 2000.
7. CCD87 - Issue 1, Marconi Applied Technology, January 2001.
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9. Sub-Electron Read Noise at MHz Pixel Rates. Craig D. Mackay, et al., Marconi Applied Technology.

Appendix A.
Analysis of current detector sub-system to determine bottleneck in frame rate.

Within the SDSU system, the bottleneck to achieving high frame rates would seem to be the down data link to the host. With a 50Mbit capacity and using 1 start bit + 16 data bits + frame recovery time, the usable bandwidth of this subsystem is restricted to 2.7 Mpix / Sec. The current CCD39 detector is 80 by 80 pixels giving a total of 6400 pixels. Using full frame readout we need a pixel rate of 6.4 Mpix / second, a value that is physically not possible with the current hardware. However, because we need only read the regions of interest the pixel rate can be reduced considerably. Considering a typical case of using 6 x 6 pixel sub-apertures and that we need 72 such sub-apertures we compute that we need only read 2592 pixels per frame. Using the 1000 frames per second required frame rate, the *average* pixel rate has been reduced to 2.6 Mpix / sec. This average value is within the capabilities of the current data link hardware. To use this full bandwidth a FIFO buffer would need to be inserted between the conversion stage and the fiber transmitter so that the peak pixel rate of 4 MPix/Sec. could be converted to an average value. A critical timing analysis of the pixel read subsystem follows to see if the required frame rate can be supported by the other elements of the SDSU hardware chain.

For each frame readout we need to transfer 40 rows into the storage area of the detector, then read 2592 pixels and skip 3808 pixels. Clear cycles would not be required as continuos readout cycles are taking place. Considering the timing we can assume 120ns per clock cycle time. This takes into account the electronic rise time of clock signals and the timing resolution of the DSP instruction set. We need 3 clock cycles for each row transfer, therefore 120ns x 3 x 40 = 14.4 ?s for the transfer. We need 3 complete serial clock cycles for each 4 skipped pixels + 80 x 3 x 120ns for parallel shifts. (3 x 120ns x 3808 pixels / 4) + (80 x 3 x 120ns) = 354.4 ?s overhead (best case) for the skipped pixels and parallel clocks. Pixel reads would use a 1?s pixel processing time (the fastest possible) to read 4 pixel values in parallel. We need to consider that the pixels of interest may not fall onto the 4 pixel boundaries in efficient manner. The worst case situation is 3 ?s / 6 pixel read and best is 2?s / 6 pixel read (obviously the most efficient would be 4 x 4 pixel sub-apertures aligned to the parallel raster giving 1?s for 4 pixel group and only 1152 pixels to read). Worst case for the current example is (3?s + 1.08?s (for clocks)) / 6 = 0.68?s / pixel. The better pixel time is (2?s + 0.72?s) / 6 = 0.453 ?s/pixel. We need 2592 pixels so time for reading overhead is 1762.5 ?s worst case and 1174 ?s better case. The frame rate is then 472 Hz worst case and 654 Hz best case for 6 x 6 sub-apertures giving 1.22 Mpix under worst case and 1.70 Mpix under best conditions. This assumes a FIFO buffer implemented in the SDSU hardware to convert the peak pixel rate (4 Mpix/sec.) into an average rate for transmission. Table 1 indicates expected frame and pixel rates for given sub-apertures on the current hardware configuration.

Sub Aperture	Pixels Read	Read Time (?s)	Pixels Skipped	Skip Time (?s)	Parallel Time (?s)	Frame rate (/ Sec)	Av. Pixel Rate (Mpix/Sec)
3 x 3	648	331	5752	518	43.2	1120	0.753
4 x 4	1152	588	5248	472	43.2	906	1.043
6 x 6	2592	1392	3808	343	43.2	562	1.456
8 x 8	4608	2350	1792	161	43.2	391	1.802
Full frame	6400	2176	0	0	43.2	451	2.886

Table 1. Theoretical maximum pixel rates available with 72 sub-apertures.

Conclusions from analysis.
Given the actual hardware configuration of the SDSU controller, the primary limiting element to the required frame rate is the pixel conversion rate. Since the detector is physically limited to 4 output ports, only by reducing the time taken to convert a pixel will the target frame rate be achieved with this detector. The required pixel processing time to achieve the 1KHz frame rate, while using the timing analysis values for clocks as previously computed, is 350ns / pixel. This would imply a 150ns x 2 integration period + settling time within the video processor. An addition limitation is imposed by the data down link bandwidth. This forces the effective pixel conversion time to be greater than 1.48 ?s because no data buffering is provided by SDSU. Assuming that areas of interest are read out, a simple FIFO buffer placed between the converters and fiber transmitter would allow the pixel burst rate to be converted to an average rate that can be handled by the current data down link hardware. The values computed here are within believable tolerance to those published in reference 1.