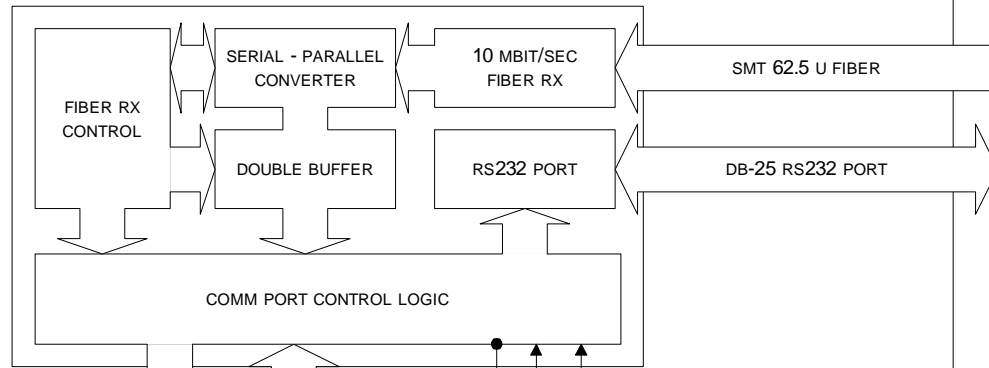


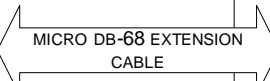
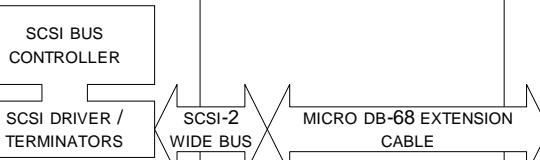
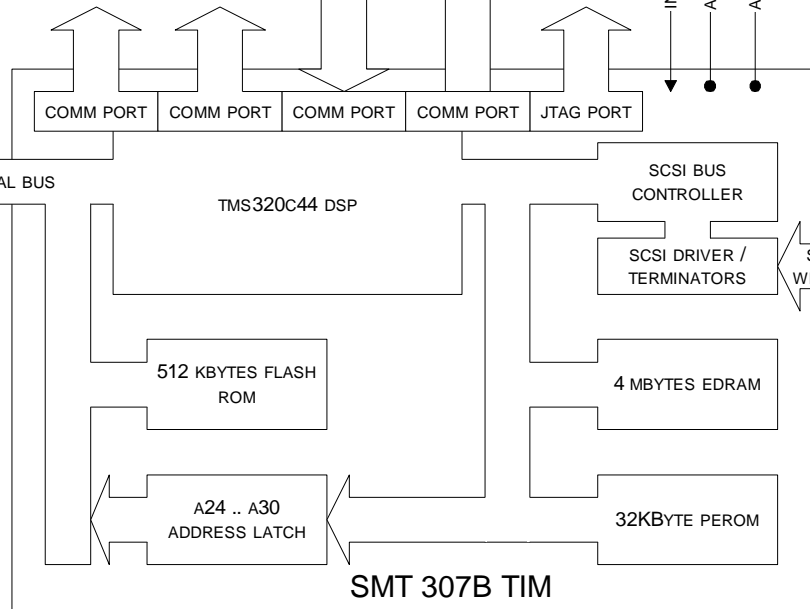
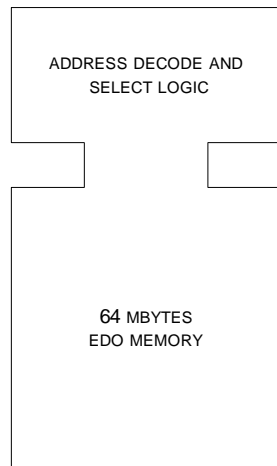
ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
General Arrangement		
Date: 25/3/98	Rev: 0.1	Author: pcm

3 SLOT TIM MOTHER BOARD
WITH POWER SUPPLY

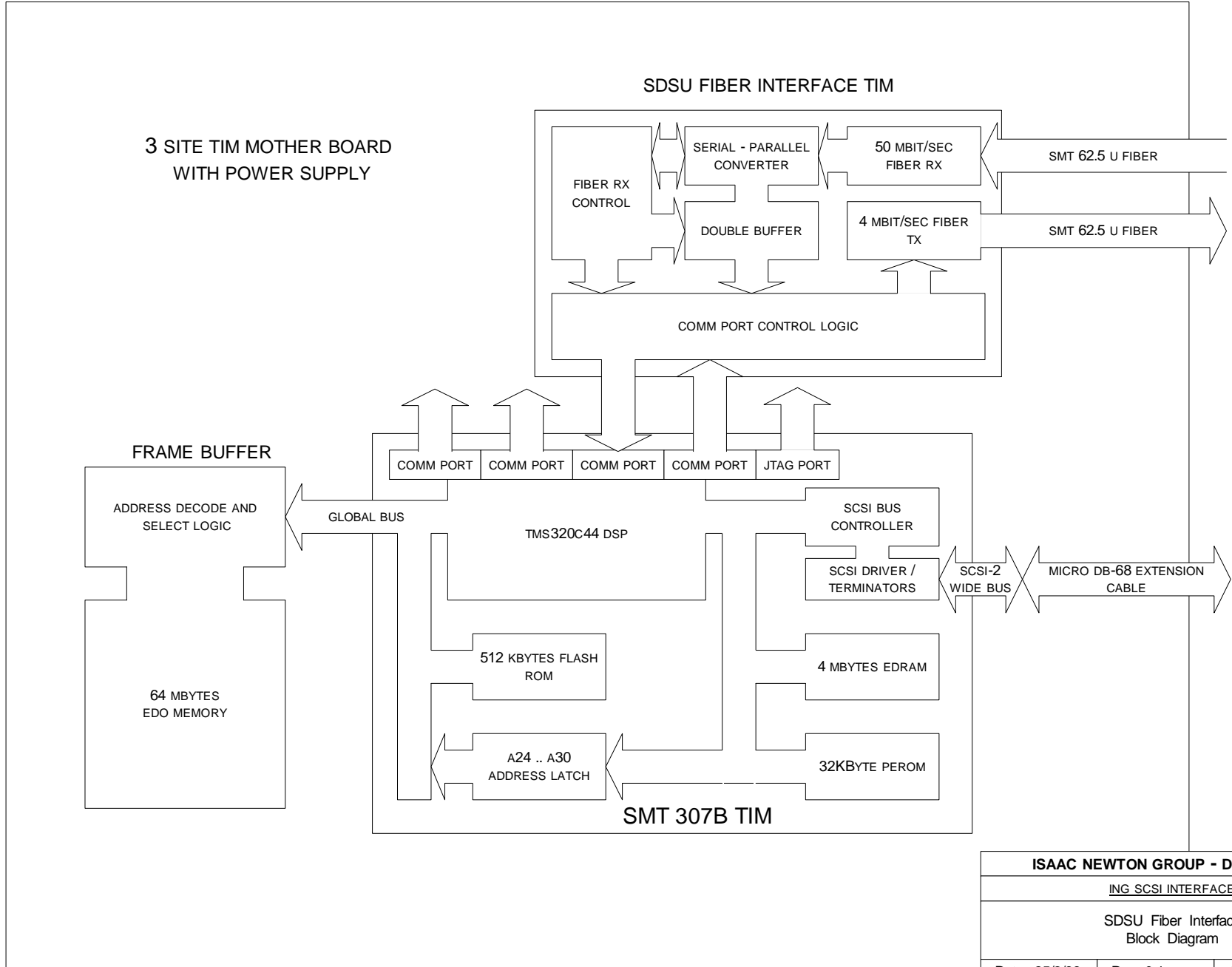
RGO FIBER INTERFACE TIM



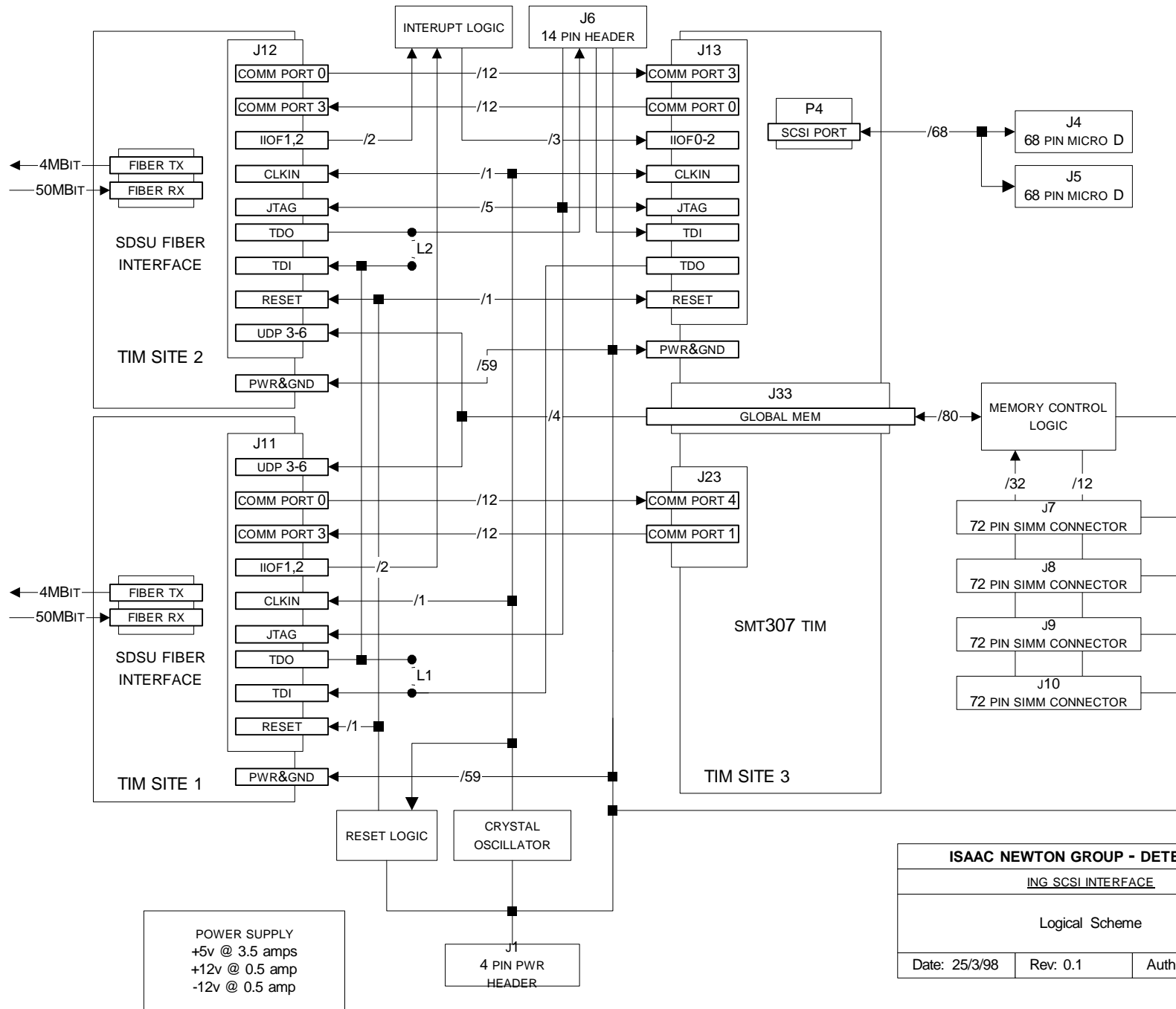
FRAME BUFFER



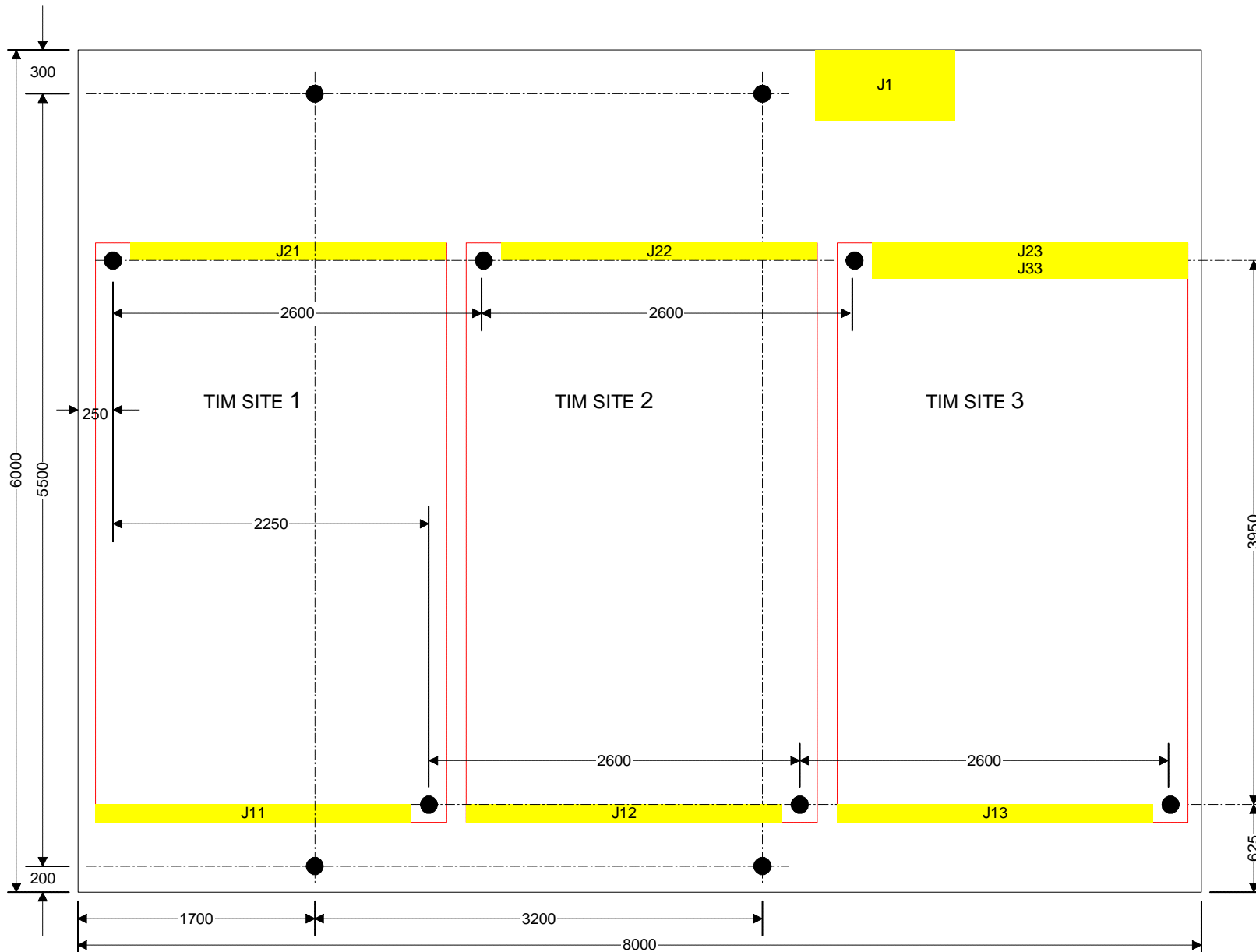
ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
RGO Fiber Interface Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm



ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
SDSU Fiber Interface Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm

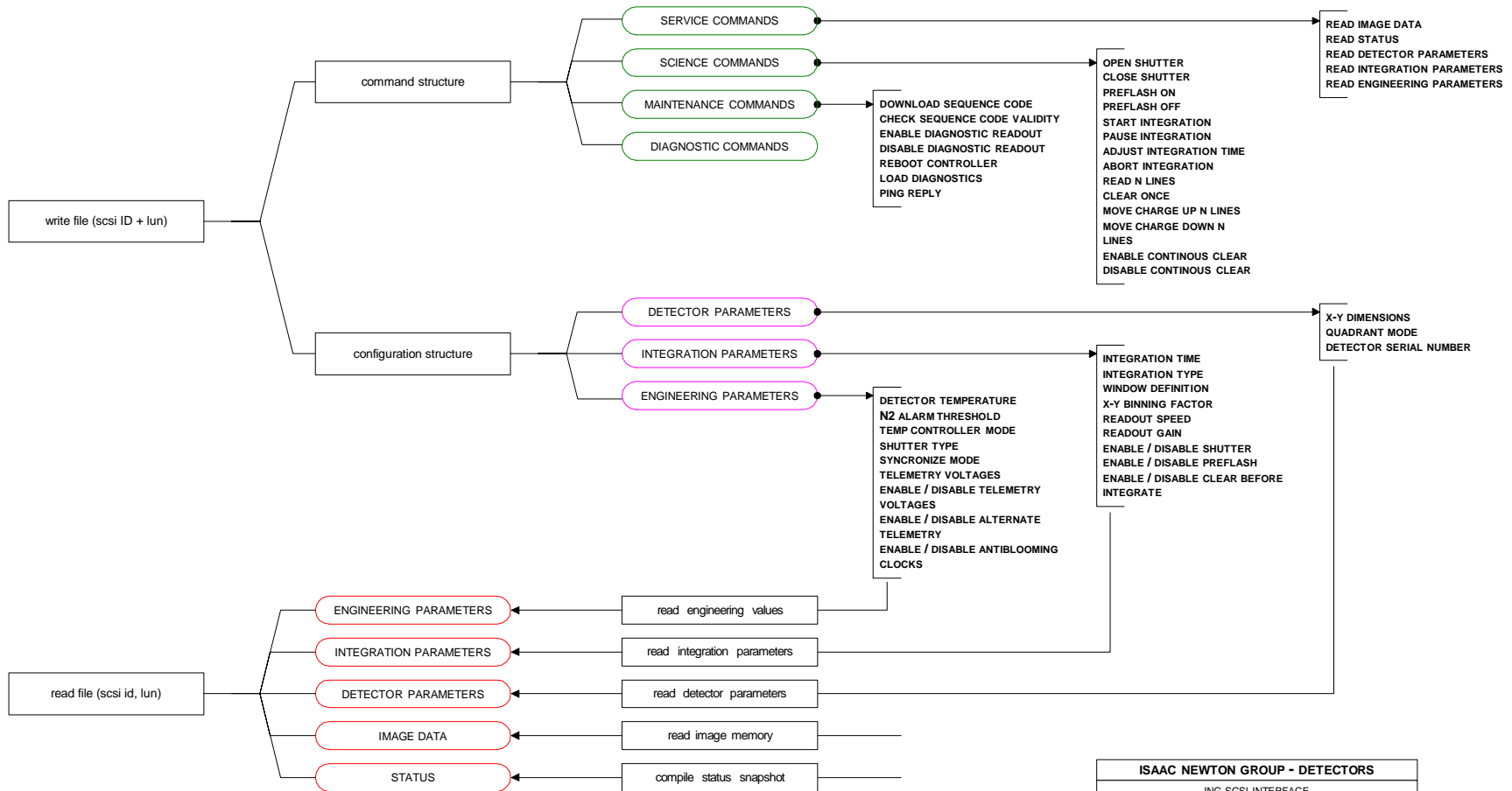


ISAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
Logical Scheme		
Date: 25/3/98	Rev: 0.1	Author: pcm



all dimensions in thou's
of an inch

ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Mother Board Mechanical Layout		
Date: 25/3/98	Rev. 0.1	Author: pcm



DOWNLOAD SEQUENCE CODE
 CHECK SEQUENCE CODE VALIDITY
 ENABLE DIAGNOSTIC READOUT
 DISABLE DIAGNOSTIC READOUT
 REBOOT CONTROLLER
 LOAD DIAGNOSTICS
 PING REPLY

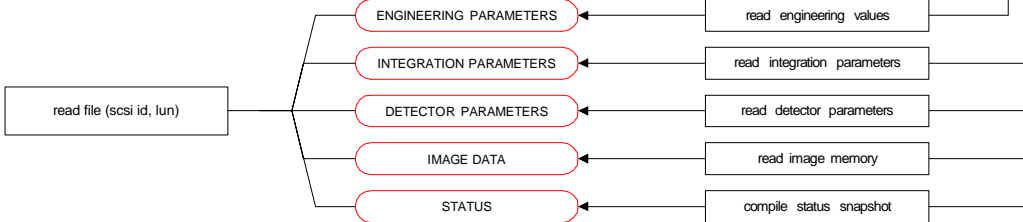
OPEN SHUTTER
 CLOSE SHUTTER
 PREFLASH ON
 PREFLASH OFF
 START INTEGRATION
 PAUSE INTEGRATION
 ADJUST INTEGRATION TIME
 ABORT INTEGRATION
 READ N LINES
 CLEAR ONCE
 MOVE CHARGE UP N LINES
 MOVE CHARGE DOWN N LINES
 ENABLE CONTINUOUS CLEAR
 DISABLE CONTINUOUS CLEAR

READ IMAGE DATA
 READ STATUS
 READ DETECTOR PARAMETERS
 READ INTEGRATION PARAMETERS
 READ ENGINEERING PARAMETERS

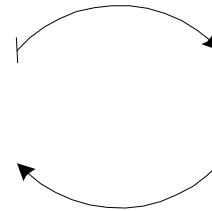
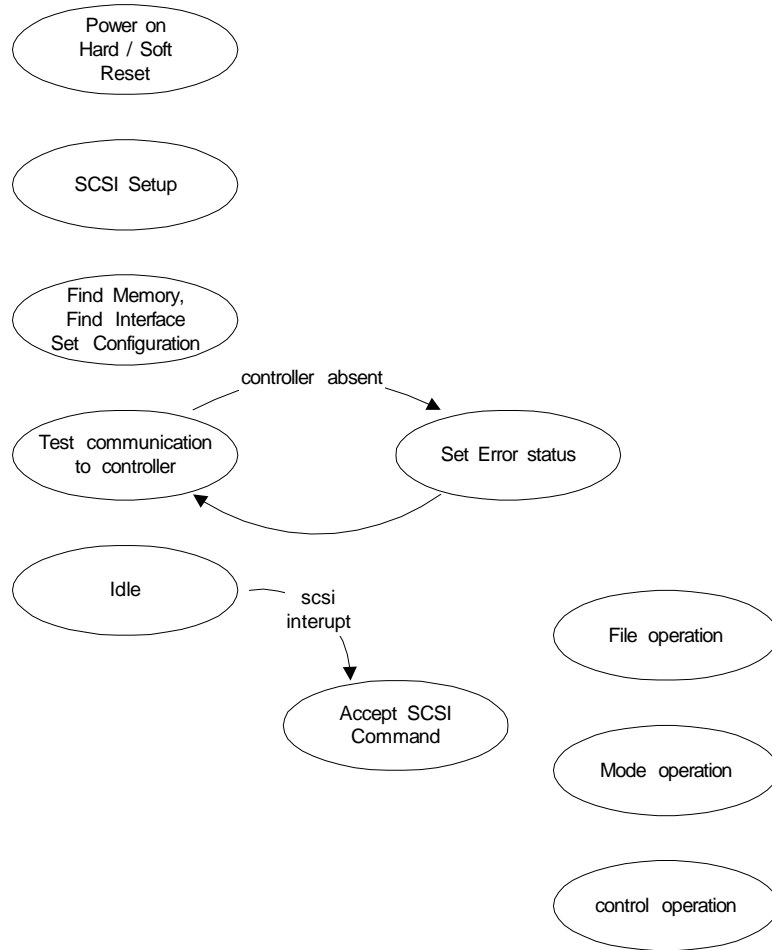
DETECTOR TEMPERATURE
 N2 ALARM THRESHOLD
 TEMP CONTROLLER MODE
 SHUTTER TYPE
 SYNCHRONIZE MODE
 TELEMETRY VOLTAGES
 ENABLE / DISABLE TELEMETRY
 VOLTAGES
 ENABLE / DISABLE ALTERNATE
 TELEMETRY
 ENABLE / DISABLE ANTIBLOOMING
 CLOCKS

INTEGRATION TIME
 INTEGRATION TYPE
 WINDOW DEFINITION
 X-Y BINNING FACTOR
 READOUT SPEED
 READOUT GAIN
 ENABLE / DISABLE SHUTTER
 ENABLE / DISABLE PREFLASH
 ENABLE / DISABLE CLEAR BEFORE
 INTEGRATE

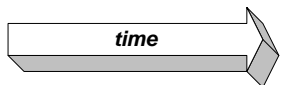
X-Y DIMENSIONS
 QUADRANT MODE
 DETECTOR SERIAL NUMBER



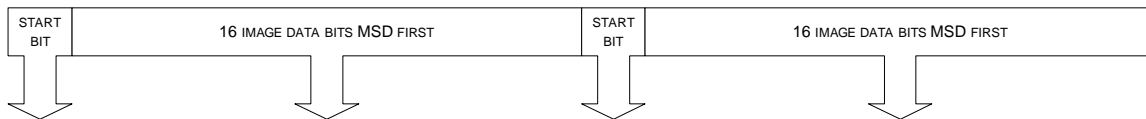
ISAAC NEWTON GROUP - DETECTORS		
<u>ING_SCSI_INTERFACE</u>		
Software Command Set and Hierarchy		
Date: 25/3/98	Rev: 0.1	Author: pcm



ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
Software Logical Structure		
Date: 25/3/98	Rev: 0.1	Author: pcm

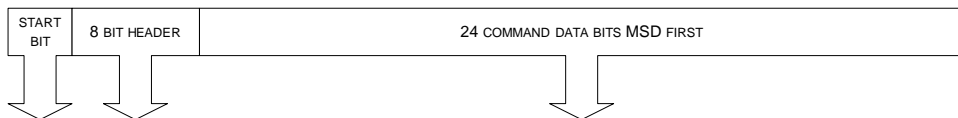


SDSU DATA PROTOCOL



50 Mbit / sec Scrambled NRZ

SDSU MESSAGE PROTOCOL



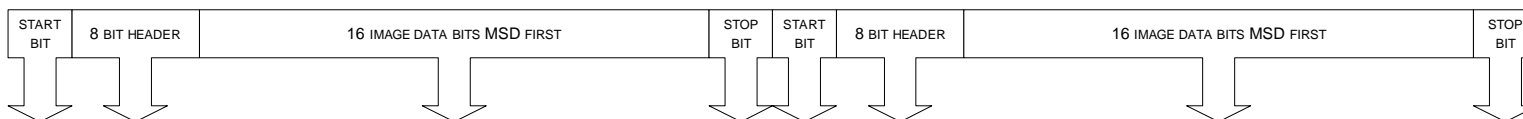
4 Mbit / sec Scrambled NRZ

SDSU MESSAGE PROTOCOL



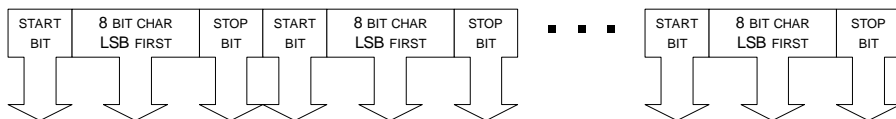
50 Mbit / sec Scrambled NRZ

RGD DATA PROTOCOL



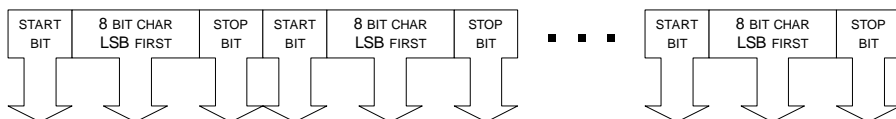
**Manchester encoded
10 Mbit / sec**

RGD COMMAND PROTOCOL



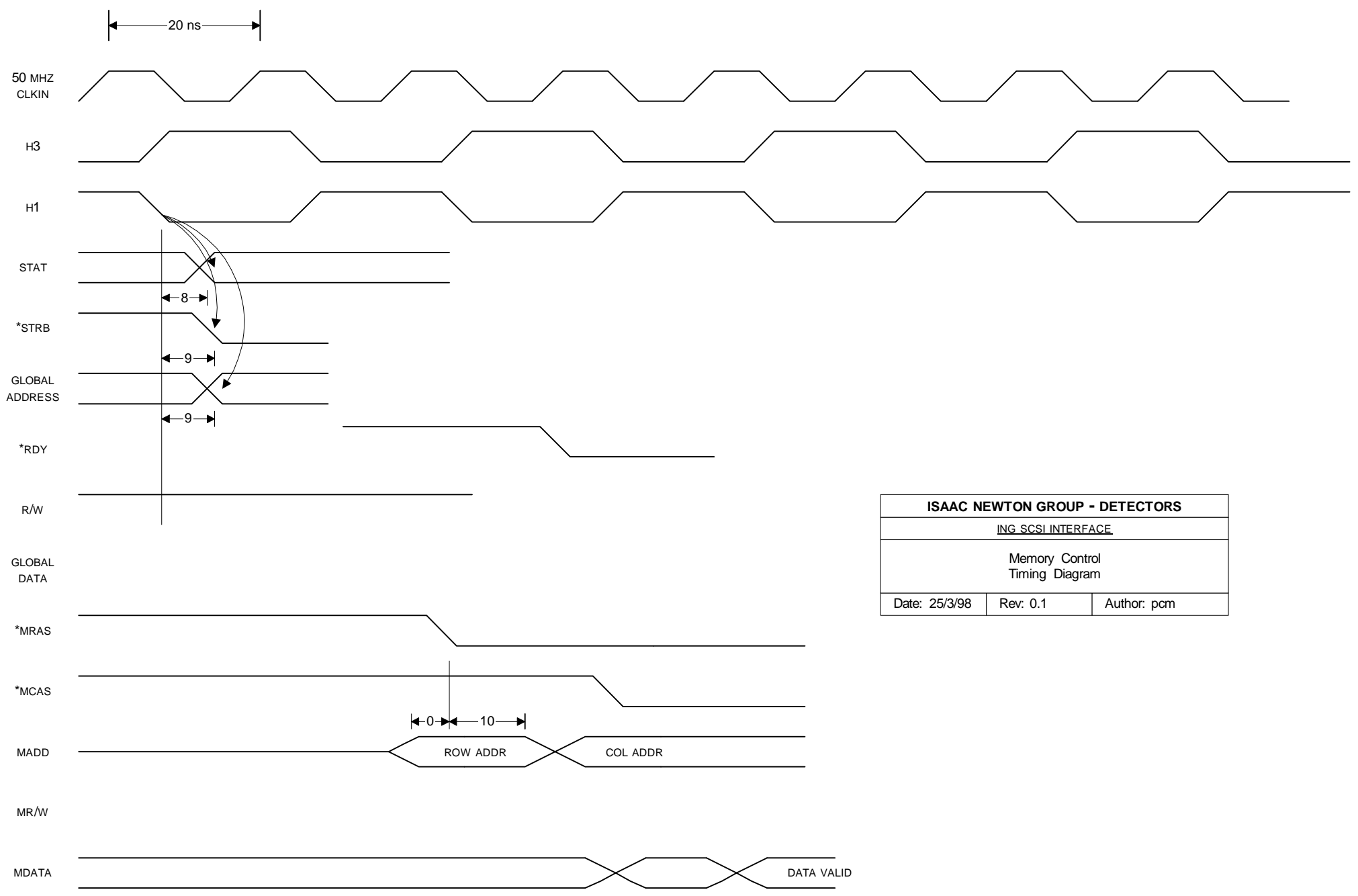
RS232 9600 baud Multi character / variable length

RGD MESSAGE PROTOCOL

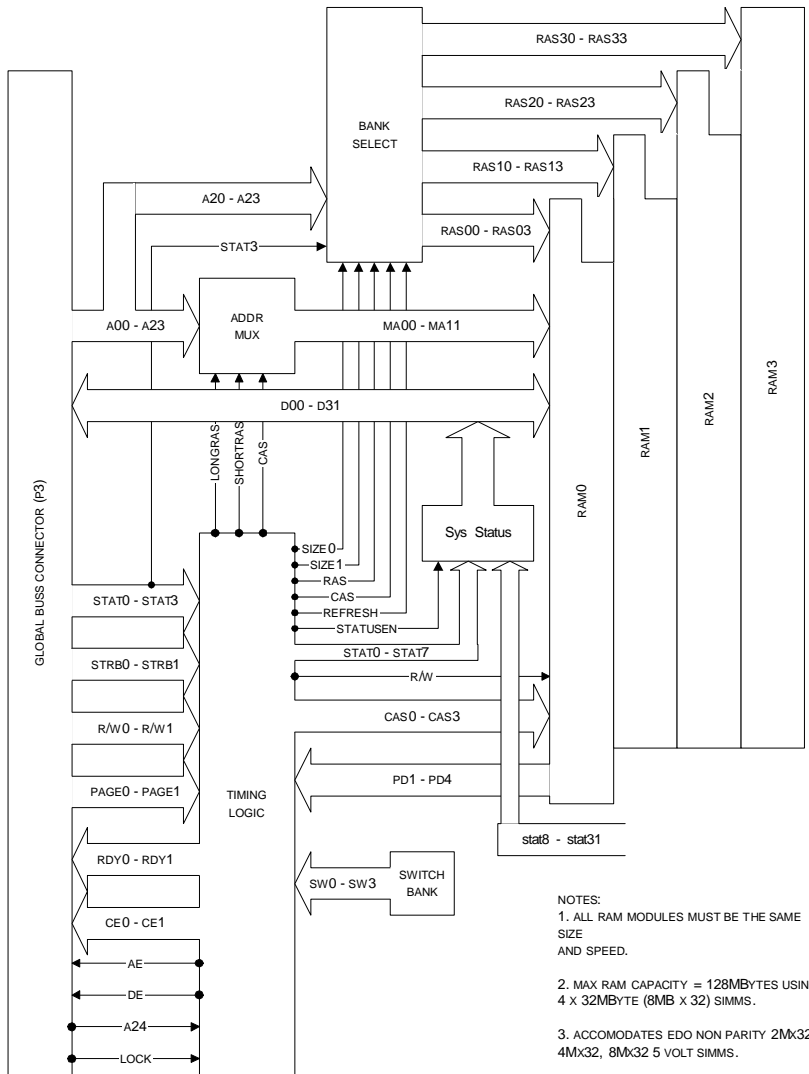


RS232 9600 baud Multi character / variable length

ISAAC NEWTON GROUP - DETECTORS		
ING_SCSI_INTERFACE		
Software Fiber Protocols		
Date: 25/3/98	Rev: 0.1	Author: pcm



ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Memory Control Timing Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm

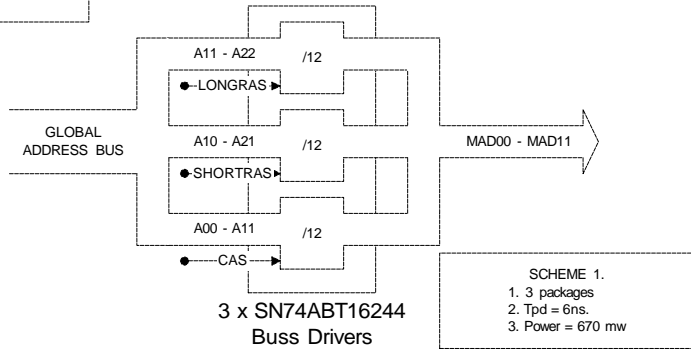


- NOTES:
1. ALL RAM MODULES MUST BE THE SAME SIZE AND SPEED.
 2. MAX RAM CAPACITY = 128MBYTES USING 4 x 32MBYTE (8MB x 32) SIMMS.
 3. ACCOMODATES EDO NON PARITY 2Mx32, 4Mx32, 8Mx32 5 VOLT SIMMS.
 4. LOCK SIGNAL IS USED BY SOFTWARE REFRESH ACCESS
 5. A24 ENABLES MEMORY BANK WHEN 8Mx32 SIMMS USED

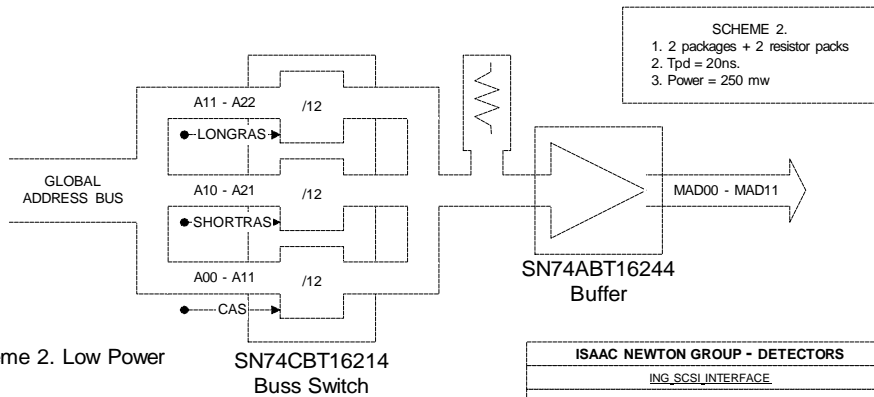
ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
Memory Control Logic Block Diagram		
Date: 25/3/98	Rev: 0.1	Author: pcm

SIZE MBYTE	ADDRESS SPACE	32MBit SIMM	16MBit SIMM	8MBit SIMM
8	8000000 - 81FFFFFF	J7	J7	J7
16	8200000 - 83FFFFFF			J8
24	8400000 - 85FFFFFF		J8	J9
32	8600000 - 87FFFFFF			J10
40	8800000 - 89FFFFFF	J8	J9	
48	8A00000 - 8BFFFFFF			
56	8C00000 - 8DFFFFFF			
64	8E00000 - 8FFFFFFF			
72	9000000 - 91FFFFFF	J9		
80	9200000 - 93FFFFFF			
88	9400000 - 95FFFFFF			
96	9600000 - 97FFFFFF			
104	9800000 - 99FFFFFF	J10		
112	9A00000 - 9BFFFFFF			
120	9C00000 - 9DFFFFFF			
128	9E00000 - 9FFFFFFF			

Scheme 1. High Speed



Scheme 2. Low Power



ISAAC NEWTON GROUP - DETECTORS		
ING SCSI INTERFACE		
Memory Control Logic Address Mux		
Date: 25/3/98	Rev: 0.1	Author: pcm

RAS00

ISAAC NEWTON GROUP - DETECTORS		
<u>ING SCSI INTERFACE</u>		
Memory Control Logic Address Decode		
Date: 25/3/98	Rev: 0.1	Author: pcm