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INGRID - FANOUT BOARD -TECHNICAL DESCRIPTION

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INGRID HAWAII FANOUT BOARD TECHNICAL DESCRIPTION

This note gives a detailed technical description of the fanout board as used with the HAWAII array in ING's new infra red imager INGRID. This board allows independent control of each of the four quadrants of the HAWAII array. It should, in theory, be possible to fast window on one quadrant while still integrating on the other three quadrants.
This option has yet to be tested in practice.

Board Layout

The board's L shape was determined by the space available inside INGRID itself. A rectangular shaped board would not have fitted inside.
The board is of a muli-layer construction, in fact, it has ten layers in total. The main reasoning behind so many layers is the fact that the board has to operate at temperatures below 70K and also has to suffer repeated thermal cycling to get to such low temperatures. The board therefore consists of many ground and power planes which are useful for shielding low level signals but more importantly in this case ensure that there are no thermal gradients across the board when it is thermal cycling. The board is constructed from standard PCB materials (PTFE etc was too expensive!!!) so the addition of extra layers and planes helps to protect the board during the cool down and warm up process. The board layout was also designed with the idea of separating as much as practically possible the low level analogue signal lines from the clock lines. To this end all the clocks come into the board on connector J2 ,a 37 way MDM, on one side of the board whereas all the outputs and analogue biases enter/leave the board via a connector at the other side of the board, J1, a 31 way MDM. These signal lines are also separate from each other with the clocks laid out between the digital power and ground planes and the signals between the bias and power planes.

The 1o layers are laid out as follows:-

?? Thermal Layer
?? Clock Signals Layer
?? Digital Power Layer
?? Clock Signals Layer
?? Digital Ground Layer
?? Signals Layer
?? High1,2,3,4 Power Layer - separated on layer
?? Signals Layer
?? Analogue Ground Layer
?? Thermal Layer

There is an option to make a link connection between the AGND layers and the DGND layer. The thermal layers which are top and bottom can also be connected to the ground planes as well if this option is required. The thermal grounds were implemented to reduce the emissivity of the board and also to reduce the thermal gradients across the board.
The board also comes with holes all around the edge and near the array mount to allow a radiation box to be build around the fanout board itself.

J1 socket pinout

Analogue signal lines and bias supplies

Connector Pin Number	Fanout Board Signal Name
1	
2	VRESET
3	BIASPOWER
4	BIASGATE
5	AGND
6	OUT4 (goes to AGND on board)
7	OUT4+
8	OUT3 Shield (goes to AGND on board)
9	OUT3+
10	OUT2 Shield (goes to AGND on board)
11	OUT2+
12	OUT1 Shield (goes to AGND on board)
13	OUT1+
14	AGND
15	HIGH2
16	HIGH1
17	HIGH4
18	HIGH3
19	
20	Thermal Ground Plane
21	
22	AGND
23	OUT4-
24	AGND
25	OUT3-
26	AGND
27	OUT2-
28	AGND
29	OUT1-
30	AGND
31	Bias Shield (goes to AGND on board)

J2 socket pinout

Clock lines and digital supply

Connector Pin Number	Fanout Board Signal Name
1	DGND
2	VDD
3	
4	CLOCK SHIELD (goes to DGND on board)
5	LINE4
6	LINE3
7	LINE2
8	LINE1
9	CLOCK SHIELD (goes to DGND on board)
10	LSYNC4
11	LSYNC3
12	LSYNC2
13	LSYNC1
14	CLOCK SHIELD (goes to DGND on board)
15	PIXEL4
16	PIXEL3
17	PIXEL2
18	PIXEL1
19	DGND
20	DGND
21	VDD
22	VDD Shield (goes to DGND on board)
23	RESET4
24	RESET3
25	RESET2
26	RESET1
27	
28	READ4
29	READ3
30	READ2
31	READ1
32	CLOCK SHIELD (goes to DGND on board)
33	FSYNC4
34	FSYNC3
35	FSYNC2
36	FSYNC1
37	DGND

J3 socket pinout

There is also a third socket fitted to the fanout board which is used for service functions such as temperature monitoring of the board itself and control of the on board LED which can be used for testing of the array without the use of external radiation sources.

Connector Pin Number	Fanout Board Signal Name
1	
2	
3	
4	
5	
6	FLASH LED+
7	FLASH LED-
8	DIODE TEMP+
9	DIODE TEMP-

Theory of Operation

The fanout board has been designed to operate the array in all the combinations possible to run the array except using the on board source follower FETs. These FETS (HAWAII pins SOURCE1...4 and DRAIN Pins1...4) are connected directly together and then taken directly to AGND. These on board FETS are known to be a source of glow during integration and it was thought best to by pass these for INGRID operation. The BUS1...4 lines (the GATES of the on board FETs) are brought out external to the array and connect directly to external JFET source follower circuits. The external FET design allows for both N-type or P-type FETs to be used.

P-type FET operation

To operate with this type of FET requires that the following components be **fitted** to the board:-

1. Q2, Q4, Q6 and Q8 - all J270 FETs
2. R10,R7,R4 and R1 - all 5.11k metal film resistors

Q1,Q3,Q5,Q7,R2,R5,R8 and R11 must **NOT** be fitted to the board.

For N-type FET operation the reverse set-up to P-type operation must be implemented, that is, those components which are excluded must be fitted and those which were fitted must be excluded.

***** This configuration has yet to be tested *****

Pixel Cell Pull ups

There are two options available for pull ups to the pixel cells, either:-

1. use the on board FET circuit which is supplied with the BIASGATE and BIASPOWER supplies - this is the option as set-up at present

2. Use 200k resistors to 5V - resistors R3,R6,R9 and R12. These resistors must not be installed when using option 1 and indeed they have not bee installed for the present set-up configuration.

***** This configuration has yet to be tested *****

Pseudo - Differential Outputs

The SOURCES from the external FETs are then the outputs taken off board to be preamplified and digitised by the SDSU controller. A pseudo differential design has been implemented where a “negative output signal” is also taken off board to feed into the differential preamplifier. This negative signal is in fact a resistor to ground. The resistor value has been chosen to match the impedance looking into the source follower arrangement. This circuit arrangement does add root 2 noise to the final signal but hopefully makes up for this by its usefulness in terms of CMRR reduction.

ARRAY protection

The shorting plugs should be fitted to the fanout board at all times when not in use. 1Mohm resistors have been fitted to most lines to ensure that all lines are pulled to the same potential when not in use. Most lines also have bi polar transorbs fitted. These act like back to back zener diodes but with very much faster switch on times. The devices fitted to the fanout board at present, clip at approximately 14V. These were chosen because of worries about them clipping at much lower voltages than their rating when cold. We did not have time at RGO to optimise the tranosrb for best use. A possible upgrade option would be to replace the 14V type with a 6V type.