Tuning of L3 WFS Performance Oct 2008

The L3 WFS had shown some problems during the summer and these were addressed immediately prior to the October run. An opportunity was also taken to rationalize the controller design.

The document that describes the initial design of the L3 WFS camera can be found here: http://www.ing.iac.es:8080/~smt/WFS/DetailsOfL3WS.doc Most of its information is still relevant.

Problems encountered during Summer 2008

It was always known that the camera had less then perfect horizontal CTE. This was obvious from the single electron events that were clearly visible in high gain biases. Rather than appear as points these had small tails. During the summer the CTE experienced a sudden worsening that caused the image to slip sideways by several tens of rows rendering the camera unusable. This was addressed by various board changes in the controller, however, during this process a further problem was identified with a HV clock board that caused the controller power supply to trip when the HV clock was boosted to full amplitude. It appeared that the inrush current to the 100uF capacitor that decoupled the high voltage bus on the HV board (C9) caused this problem. Other identical boards did not show this problem. C9 was reduced to 47uF and the problem went away. The CTE problem was cured by scoping the serial clock waveforms and introducing a couple of small delays in the serial waveform tables to increase the overlaps in the clock transitions.

A further problem was identified with the camera optics that was repaired by changing the WFS code. When switching between the CCD39 and CCD60 cameras using the sliding pick off mirror there was an offset in the position of the pupil centre by about 5 pixels. The CCD60 measures 128x128 pixels in comparison to the 80x80 pixels of the CCD39. This means that the CCD60 is always readout using a window (maximum size 80x80). This is extremely convenient in that the CCD60 can be precisely aligned with the optical axis of Naomi by varying the position of this window (which is defined by two coordinates in the assembler code).

Details of Assembler Code

The source code for the L3 WFS is in /home/dspdev/L3NAOMIPCi.
The waveform tables are in the subdirectory ‘ap_boot’ in file ‘naomi_L3_clocks_voltages.asm’
The file that contains the coordinates of the window centre is also in subdirectory ‘ap_boot’ in file ‘naomi_L3_clocks_header.asm’
Once the code in the boot directory had been compiled it was then necessary to compile the various applications again and reblow the eeprom. The L3NAOMIPCi directory contains a text file describing how to do this.

Rationalisation of controller design

The boards inside the WFS controller had been modified considerably. Some of these modifications were essential , whereas others were rather experimental and reduced the compatibility of spare boards.

HV Clock Board

There are a total of 4 clock boards of two types. Two are intended for use with the QUCAMs , two for the WFS. The difference is in the value of R14 which is equal to 4K7 for the WFS controller and 6K2 for the QUCAMs. This gives extra gain for the WFS which it needs due to it not been deeply cooled and L3 gain being a strong function of temperature. No change was made to this. Two more spare boards, are now being made, one of each type.

Normal Clock Board

The initial design document included the addition of shaping capacitors to the clock outputs. This was abandoned since it slowed the readout. The clock boards are used unmodified.

Video Board.

The video boards must be modified for use with the QUCAMs and the L3 WFS. The problem is that they need to use a bias DAC on the video board to provide the non-zero substrate voltage (the science cameras all have substrate = 0V and do not need to be actively driven). The DAC output normally has a 1K resistor connected in series (R143) decoupled by a 1uF capacitor (C132). To give better substrate drive R143 was shorted out and C132 was replaced by a 22uF capacitor. Boards thus modified were labeled. Initially other mods were made to C31,C44,C93 and C74 (CDS the integration capacitors) in an attempt to speed up the readout. This never really worked so these capacitors were reverted to their default factory values.

Direct Tip-Tilt mirror drive outputs, Synch connectors and the Utility card

Experiments were done to try to use the SDSU controller to directly drive the TipTilt mirror using two DACs on an extra video board. This experiment was abandoned and one of the controllers still has external X/Y coax connectors that are not used. The controllers also carry an additional coax connector to allow their readout to be synchronized with the Pockels cell. This was never needed and the connectors are redundant. The controllers also originally contained utility cards but these were never used and are entirely redundant.

Controllers for the QUCAMs

The two WFS controllers (operational + spare/experimental) have front panel wiring that allows them to be converted quickly for use with the QUCAMs. Their front panels also contain shutter, ID and temperature connectors: all redundant for WFS use. A new front panel is being made with just the CCD connector , this will free up one of the existing front panels to allow a second QUCAM controller to be built (there are now 2

QUCAMs). Once made we will then have two of each types of L3 controller. The WFSs are Gen 2 , the QUCAMs are Gen3. If the use of both QUCAMs together on ISIS proves popular we should consider making yet another spare controller.