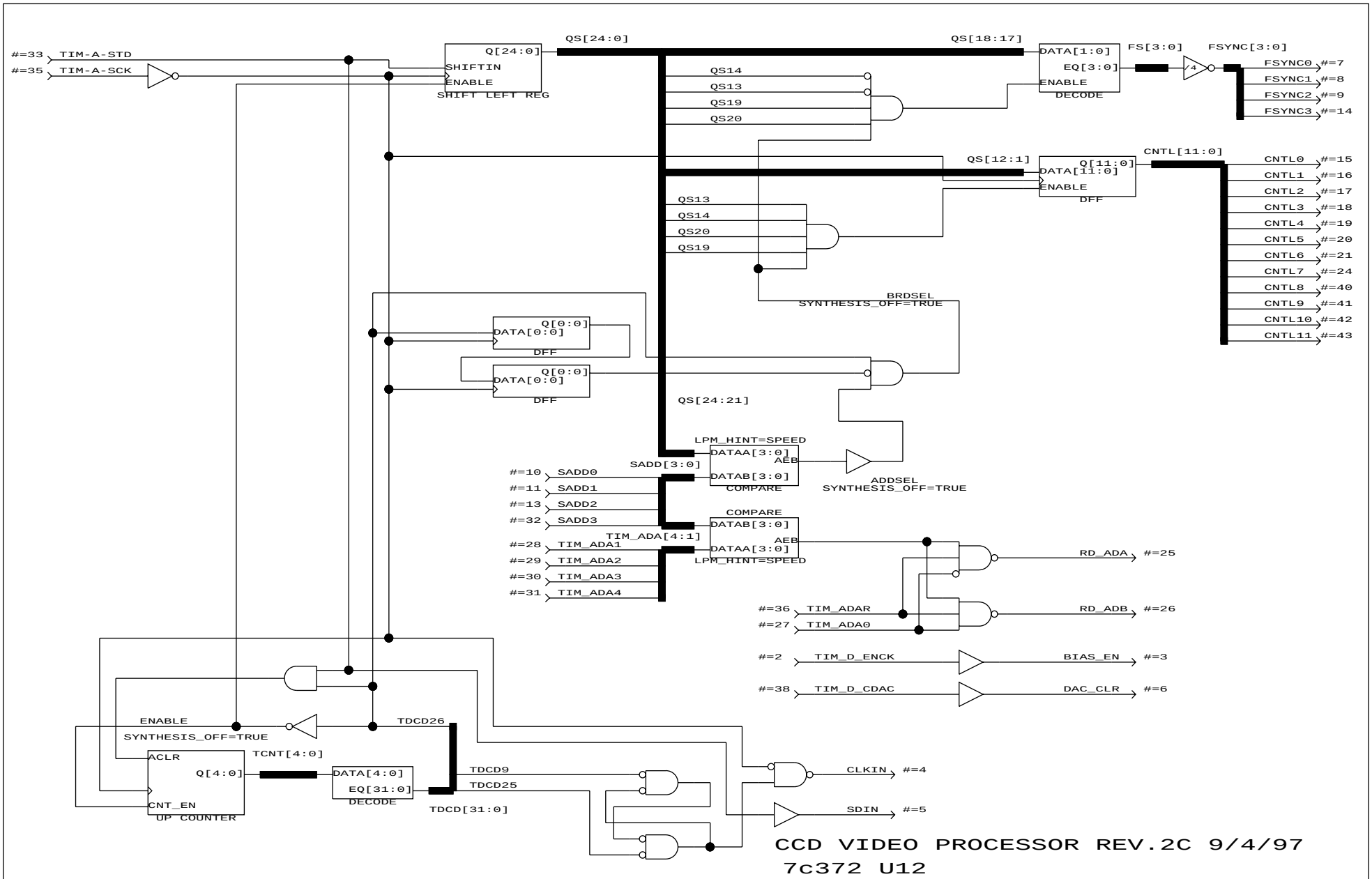
#=33 TIM-A-STD
#=35 TIM-A-SCK
Q[24:0]
SHIFTIN
ENABLE
SHIFT LEFT REG
QS[24:0]
QS[18:17]
DATA[1:0]
EQ[3:0]
ENABLE
DECODE
FS[3:0]
/4
FSYNC[3:0]
FSYNC0 #=7
FSYNC1 #=8
FSYNC2 #=9
FSYNC3 #=14
QS14
QS13
QS19
QS20
QS[12:1]
Q[11:0]
DATA[11:0]
ENABLE
DFF
CNTL[11:0]
CNTL0 #=15
CNTL1 #=16
CNTL2 #=17
CNTL3 #=18
CNTL4 #=19
CNTL5 #=20
CNTL6 #=21
CNTL7 #=24
CNTL8 #=40
CNTL9 #=41
CNTL10 #=42
CNTL11 #=43
QS13
QS14
QS20
QS19
BRDSEL
SYNTHESIS_OFF=TRUE
Q[0:0]
DATA[0:0]
DFF
Q[0:0]
DATA[0:0]
DFF
QS[24:21]
LPM_HINT=SPEED
DATAA[3:0]
AEB
DATAB[3:0]
COMPARE
ADDSEL
SYNTHESIS_OFF=TRUE
SADD[3:0]
#=10 SADD0
#=11 SADD1
#=13 SADD2
#=32 SADD3
COMPARE
DATAB[3:0]
AEB
DATAA[3:0]
LPM_HINT=SPEED
TIM_ADA[4:1]
#=28 TIM_ADA1
#=29 TIM_ADA2
#=30 TIM_ADA3
#=31 TIM_ADA4
RD_ADA #=25
#=36 TIM_ADAR
#=27 TIM_ADA0
RD_ADB #=26
#=2 TIM_D_ENCK
BIAS_EN #=3
#=38 TIM_D_CDAC
DAC_CLR #=6
ENABLE
SYNTHESIS_OFF=TRUE
TDCD26
ACLR
TCNT[4:0]
Q[4:0]
CNT_EN
UP COUNTER
DATA[4:0]
EQ[31:0]
DECODE
TDCD9
TDCD25
TDCD[31:0]
CLKIN #=4
SDIN #=5
CCD VIDEO PROCESSOR REV.2C 9/4/97
7c372 U12