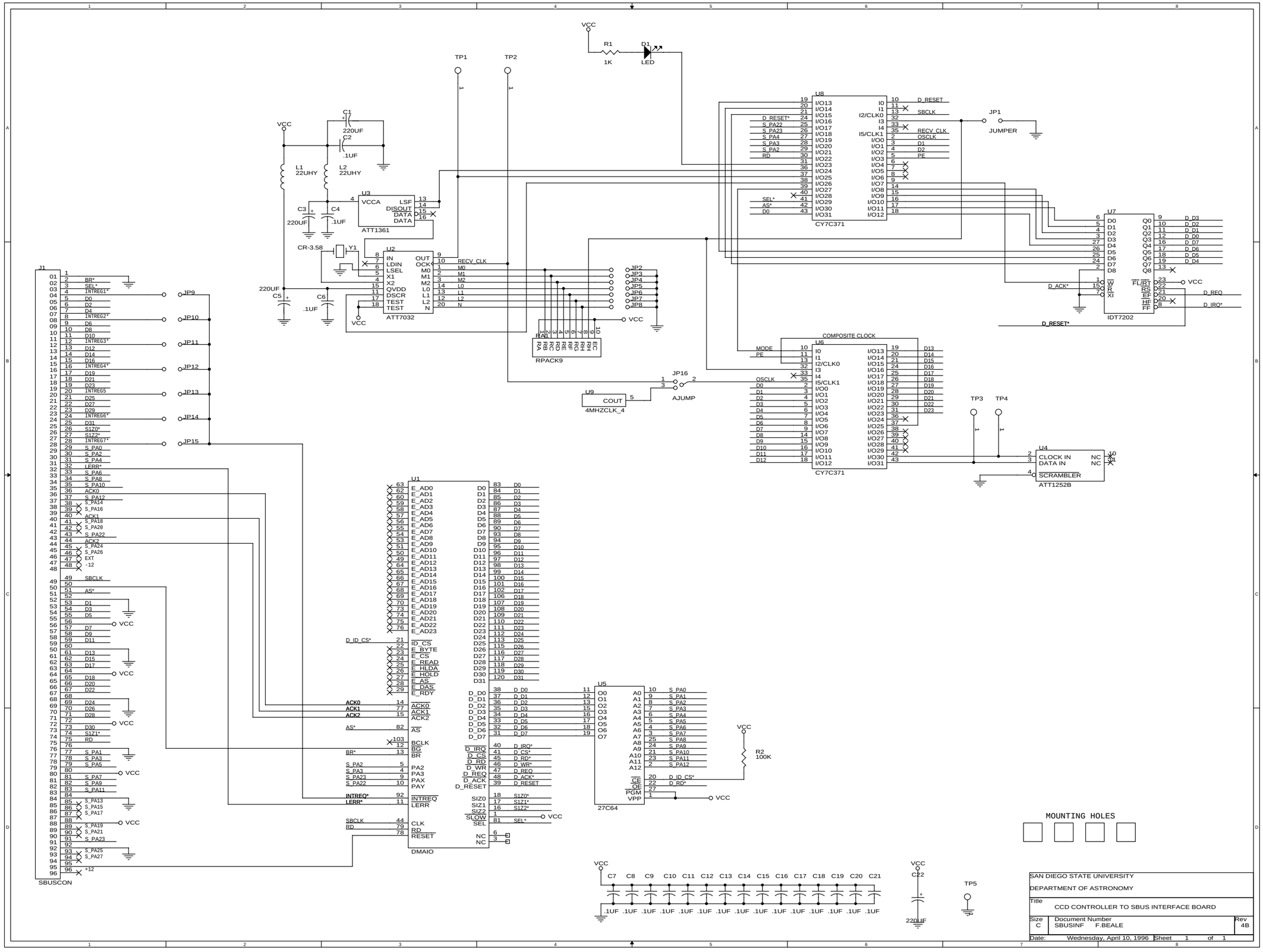
VCC
R1
1K
D1
LED
TP1
TP2
C1
220UF
C2
.1UF
L1
22UHY
L2
22UHY
C3
220UF
C4
.1UF
U3
VCCA
LSF
DISOUT
DATA
DATA
ATT1361
CR-3.58
Y1
U2
IN
LDIN
LSEL
X1
X2
QVDD
DSCR
TEST
TEST
OUT
OCK
M0
M1
M2
L0
L1
L2
N
ATT7032
C5
220UF
C6
.1UF
RECV_CLK
JP2
JP3
JP4
JP5
JP6
JP7
JP8
RA1
RPACK9
U8
CY7C371
D_RESET
SBCLK
RECV_CLK
OSCLK
D1
D2
PE
D_RESET*
S_PA22
S_PA23
S_PA4
S_PA3
S_PA2
RD
SEL*
AS*
D0
JP1
JUMPER
U7
IDT7202
D_ACK*
D_REQ
D_IRQ*
D_RESET*
COMPOSITE CLOCK
U6
CY7C371
MODE
PE
OSCLK
JP16
AJUMP
U9
COUT
4MHZCLK_4
TP3
TP4
U4
CLOCK IN
DATA IN
SCRAMBLER
ATT1252B
J1
SBUSCON
JP9
JP10
JP11
JP12
JP13
JP14
JP15
U1
DMAIO
D_ID_CS*
ACK0
ACK1
ACK2
AS*
BR*
S_PA2
S_PA3
S_PA23
S_PA22
INTREQ*
LERR*
SBCLK
RD
U5
27C64
R2
100K
MOUNTING HOLES
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
.1UF
C22
220UF
TP5
SAN DIEGO STATE UNIVERSITY
DEPARTMENT OF ASTRONOMY
Title
CCD CONTROLLER TO SBUS INTERFACE BOARD
Size C
Document Number SBUSINF
F.BEALE
Rev 4B
Date: Wednesday, April 10, 1996
Sheet 1 of 1