VIDEO PROCESSOR BOARD

This chapter describes the CCD video processor for Generation II systems. It serves two functions - processing and digitizing the video output from the CCD and supplying DC bias voltages to the CCD. It contains two identical video processing circuits that simultaneously process and digitize signals from two CCD video outputs. Two 16-bit analog-to-digital (A/D) converters are provided on the board, each with a total sample and conversion time of one microsecond. Their digital outputs are multiplexed on the backplane on dedicated A/D data pins where they are transmitted by the timing board to the host computer. The DC bias supply section of the board provides twelve separate low noise, digitally programmable voltages with a variety of voltage ranges suitable for direct connection to CCDs, as well as four offset voltages for the two video processors. A block diagram of the board is shown in Fig. 1.

THEORY OF OPERATION

The CCD output source signal, sometimes called CCD video, can be connected directly to the input SMA connector, which has a load resistor connected to ground. The load resistors R1 and R51 are mounted on fork terminals to enable the user to install and modify its value without damaging the board, and a load resistor is normally NOT installed in boards shipped. Values of 20k are normally used for Loral and SITe sensors, and a value 6.8k has been found useful with the EEV39 CCD device.

The preamp can be jumper selected to be either DC or AC coupled to the CCD. In AC coupling a 0.1μf capacitor is connected between the video signal and the non-inverting input of the preamplifier op amp to remove the large DC offset of the video signal. The preamp op amp power is then jumpered to +/-15 volts and the input offset op amp is disconnected from the preamp. For DC coupling the AC coupling capacitor is bypassed, the preamp op amp is powered from +30 volts and ground and the input offset op amp is connected to the preamp circuit. This is all accomplished with jumpers that are described below. The preamp op amp selected is an Analog Devices AD829 which is a fast, low noise voltage

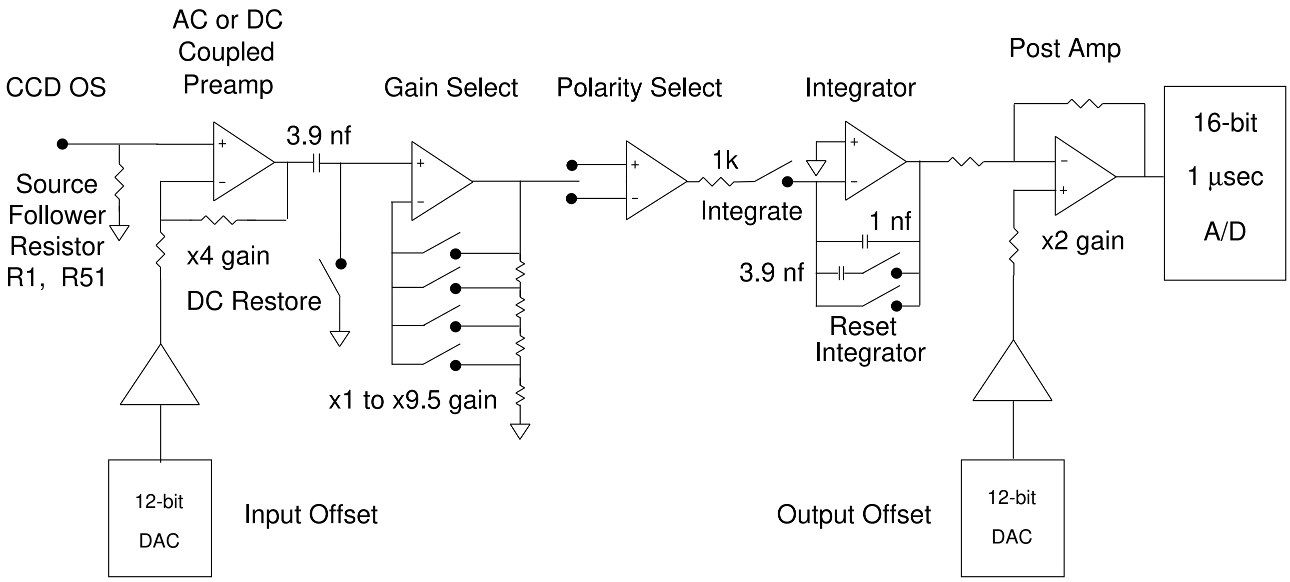

Fig. 1: Block diagram of the CCD video processor

feedback part, operated with a non-inverting gain of x4. At this gain it has a small signal bandwidth of 74 MHz, a slew rate of 70 volts per microsecond, an input voltage noise density of 1.7 nanovolts per root Hertz and an input current noise density of 1.5 picoamps per root Hertz. Although its input current noise density is larger than similar FET input parts its input voltage noise is much lower, so the output noise is lower when used with high gain CCDs that have output impedances up to several thousand kilohms.

Following the preamp is a DC restore circuit whose function is to maintain the average signal level so the op amps and analog switches are within their normal operating ranges. The DC restore switch clamps the signal level to ground every pixel before the signal is sampled, and unclamps it during the sampling. Because of the DC restore circuit the average voltage on the output of the preamp in DC coupled mode does not need to be accurately set since it will be restored to zero anyway - a convenient value is 24 volts, which simply minimizes the power dissipation on the feedback resistors. An analog switch (not shown in Fig. 1) is installed which routes this signal to the A/D converter so it can be read by the DSP for setting the input offset voltage without a voltmeter.

The gain select stage has four gain selections that are software selectable - x1.0, x2.0 x4.75 and x9.5, set by a resistor ladder. The polarity select op amp simply inverts or buffers the signal to accomplish the subtraction of (signal - baseline) which is proportional to the charge collected by the CCD pixel. It is implemented by a differential amplifier with switchable resistors on the input. The integrator is a conventional RC integrator, but with a choice of integration speeds. With the 3.9 nf capacitor switched out the integrator has an RC time constant of 1 microsecond, so will have a gain of unity for an integration time of one microsecond. This setting is suitable for operation in the fast readout mode of around 2.5 microsecond total processing time per pixel. The 3.9 nf capacitor can be switched in for a slower integration suitable for slower readouts where the stage will have unity gain for an integration time of 4.9 microsecond. The integrate analog switch is closed to enable the integrator, and the reset integrator switch is closed to discharge the integration capacitor(s) after each pixel is sampled. A simple x2 gain inverting stage follows the integrator and accepts an output offset voltage from a DAC that allows a voltage to be subtracted from the signal before the A/D conversion. The A/D converter is a fast 16-bit part that samples its input for 300 nanoseconds before its start A/D signal goes high and requires another 700 nanoseconds before its digital output data is valid. The digital output data are written to a latch when the XFER signal is clocked high, and then transmitted over the backplane when the timing board asserts the appropriate A/D selection lines.

Some of the analog switches need to be switched every pixel, and are controlled by a simple latch operating from the WRSS (write switch state) signal from the timing board that can be updated every 40 nanoseconds. Other analog switches are rarely set and are controlled from the serial data link from the timing board. The analog switches are all Siliconix DG611 parts with a low control logic input signal closing the switch. These are fast, low ON resistance, and low charge dumping parts that unfortunately can be easily damaged if their input voltage ranges are exceeded. This has necessitated the insertion of several protection diodes in the circuit and the operation of the op amps driving the switches from unconventional voltages, both to limit the voltage range on the switches and to lower power dissipation. Both video processors on the same board have the same timing. These are the following -

TABLE 1 - Fast timing analog switch definition

Function	Schematic name	Timing	Description
Reset integrator	RESET	SS0	Low to reset the integrator
DC Restore	DC-REST	SS1	Low to DC restore
Polarity -	POL-	SS2	Low for inverting signal integration
Polarity +	POL+	SS3	Low for non-inverting signal integration
Integrate	INTEG	SS4	Low to integrate
Start A/D	A/D	SS5	Low to high transition to start A/D convert
Transfer A/D	XFER	SS6	Low to high transition to transfer data from A/D to latch

Other analog switches are rarely switched, usually only while configuring of the system. They are controlled from serial words sent from the timing board, the same mechanism used to update DAC voltages. They can be set to different values on the two video processors. These are as follows -

TABLE 2 - Configuration analog switch definition

Function	Schematic name	Data value	Description
Gain ch. A, x9.5	GAIN-A-0	D0	Low to enable x9.5 gain on ch. A
Gain ch. A, x4.75	GAIN-A-1	D1	Low to enable x4.75 gain on ch. A
Gain ch. A, x2.0	GAIN-A-2	D2	Low to enable x2.0 gain on ch. A
Gain ch. A, x1.0	GAIN-A-3	D3	Low to enable x1.0 gain on ch. A
Gain ch. A, x9.5	GAIN-B-0	D4	Low to enable x9.5 gain on ch. B
Gain ch. A, x4.75	GAIN-B-1	D5	Low to enable x4.75 gain on ch. B
Gain ch. A, x2.0	GAIN-B-2	D6	Low to enable x2.0 gain on ch. B
Gain ch. A, x1.0	GAIN-B-3	D7	Low to enable x1.0 gain on ch. B
Int. speed, Ch. A	INTEGRATE-A	D8	High for fast integrate speed, ch. A
Int. speed, Ch. B	INTEGRATE-B	D9	High for fast integrate speed, ch. B
Rd preamp, ch. A	ADJ-ENAB-A	D10	Read preamp voltage on A/D, Ch. A
Rd preamp, ch. B	ADJ-ENAB-B	D11	Read preamp voltage on A/D, Ch. B

The 12-bit DAC circuits for the DC bias supplies receive their digital data words over serial lines from the PAL U12 that converts 24-bit words from the timing board's synchronous serial interface (SSI) to 16-bit serial words routed to each DAC on the video board. Two of the DACs have bipolar outputs from +10 to -10 volts, and two of them have unipolar outputs from +2.5 to +10 volts. This is determined by the polarity and values of the reference inputs to the DACs. The outputs of the DACs are heavily filtered before going to the non-inverting inputs of low noise op amps. Four of these voltages are used on the video processor board for offset control. The remaining twelve outputs are passed through DG405 switches whose function is to be open whenever there is reason to suspect that the voltages are not set to their proper values or the power supply to the controller has failed. The control line TIM-D-ENCK controlled by the timing board is set high to close the switches and allow the DC bias voltages to propagate to the output connector. RC filters then decouple any remaining noise on the lines. The table of available voltages follows, where names are assigned to some of the DC bias signals used to operate a quad readout EEV39 CCD with two video processor boards. A wiring list named EEV39.txt is available for the EEV39 sensor that maps the pins on the controller boards to the sensor pins, along with DSP timing board readout code named timEEV39.asm. The input offset voltage are routed to the offset circuit of the DC coupled preamp and determine the voltage levels routed to the gain amplifier, while the output offset voltage goes to the op amp directly in front of the A/D.

TABLE 3 - DC bias voltages definition

DB25 pin #	Function	Voltage range	DAC address	Description
	INPUT-OFFSET-A		$0c0xxx	Input offset, ch. A
	OUTPUT-OFFSET-A		$0c4xxx	Output offset, ch. A
	INPUT-OFFSET-B		$0c8xxx	Input offset, ch. B
	OUTPUT-OFFSET-B		$0ccxxx	Output offset, ch. B
1	VOD-A	+7.5 to +30	$0d0xxx	Output Drain, ch. A
2	VOD-B	+7.5 to +30	$0d4xxx	Output Drain, ch. B
3	VRD-A	+5.0 to +20	$0d8xxx	Reset Drain, ch. A
4		+5.0 to +20	$0dcxxx	not used
5		+5.0 to +20	$0e0xxx	not used
6		+5.0 to +20	$0e4xxx	not used
7		+5.0 to +20	$0e8xxx	not used
8		+5.0 to +20	$0ecxxx	not used
9		-5.0 to +5.0	$0f0xxx	not used
10		-5.0 to +5.0	$0f4xxx	not used
11	VOG-A	-10 to +10	$0f8xxx	Output Gate, ch. A
12	VOG-B	-10 to +10	$0fcxxx	Output Gate, ch. B
14				+15 volts power
15				-15 volts power
13,16,17,18,19,20,21,22,23,24,25				Ground

BOARD LAYOUT AND POWER REGULATION

An engineering drawing showing the layout of the parts are available in postscript format as filename vpCCDparts3B.lpsf. A schematic of the board is available in postscript format with a filename of vpCCDsch3B.lpsf. Both files are sized to be printed on 11x17 inch paper, though the user can adjust scaling parameters at the beginning of the file to print on other sized paper.

The layout of the principal components of the video processor board is shown in Fig.2. Two of the four coaxial connectors on the left of the board are SMA connectors (the ones with threads), used to connect to the CCD, and two of them are SMB connectors (the push-on type), connected to the output of the preamplifier for inspection of the CCD video waveform with an oscilloscope. The CCD source follower load resistors are mounted on fork terminals for easy user configuring, behind the output

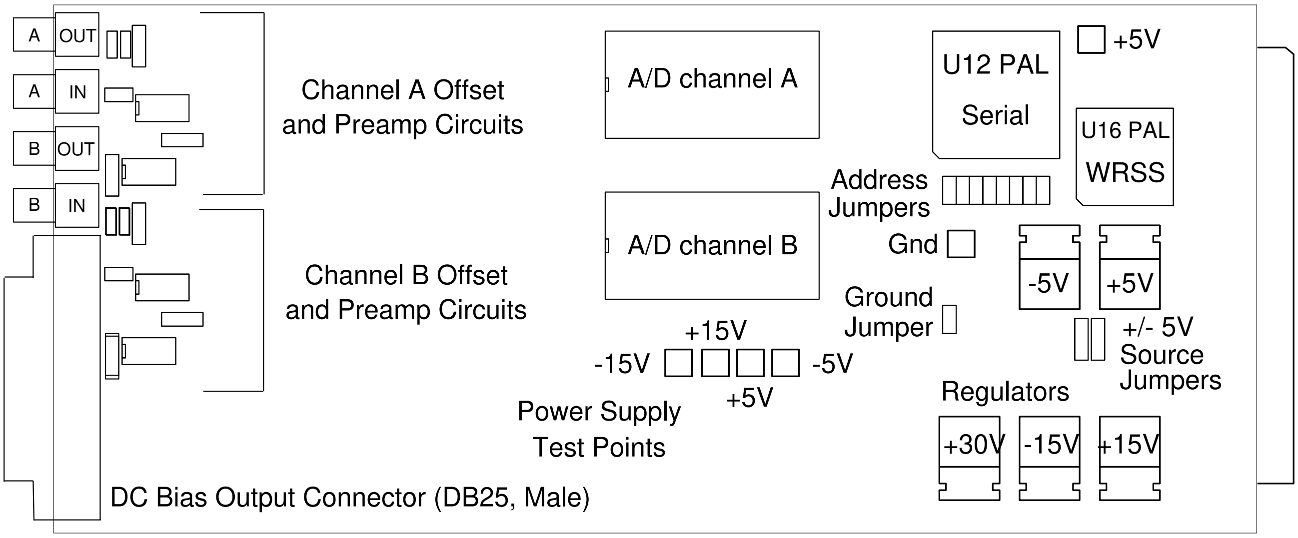

Fig 2: Components layout for the video processor board

SMB connector for channel A and behind the input SMA connector for channel B. The user should install appropriately sized resistors in these fork terminals. The jumpers required to switch from AC to DC coupling surround the two op amps of the preamplifier and input offset circuits, and are shown in greater detail in Fig. 3.

The DC bias voltages are output on the large 25-pin DB connector at the lower left of the board following the pinout of Table 3. Power supply test points are provided below the A/D converters near the center of the board. These monitor the analog power supply voltages that power the op amps and A/D converters on the board, as derived from the on-board regulators. The user can conveniently probe these test points to ensure that the voltages are within range. The tolerances required by the A/D converter to operate within specifications are pretty tight: +/- 0.50 volts on the two fifteen volt supplies and +/- 0.25 volts on the two five volt supplies. Trim resistors R156 and R157 are located in the regulator circuit for adjusting these voltages to be within range, which is done for each board after the components are installed. There is an additional test point in the upper right hand corner of the board that connects to the digital five volts supply, which is not regulated on this or any other controller board. The theoretical tolerance of the digital supply is +/- 0.25 volts, though its usually best to set it to +5.05 volts on the power control board test point. A test point does not exist for the +32 volt supply.

Five on-board regulators provide the analog voltages for the board. They are all low overhead regulators to permit low power dissipation on the board, but since the A/D converters have tight tolerances on their supply lines users supplying their own system power should pay careful attention that the overhead requirements of the regulator and that the circuit is trimmed to meet the voltage specification of the A/D converters. The voltages supplied to the video board are normally set at +/- 16.5 volts to allow adequate overhead. The A/D converter and some of the op amps require +/- 5.0 volt power. It can be derived either from the +/- 16.5 volts supply, or from the +/- 6.5 volts supplied on the backplane. Lower power dissipation is attained if power is supplied the +/- 6.5 volts lines, and systems containing large number of video processor boards should be configured in this way. However, care should be taken when providing +/- 6.5 volts power on the backplane because they are routed on the backplane pins B30 and C28 that are narrow trace signal lines. Systems supplied after March 1998 are supplied with switcher power supplies that provide +/- 6.5 volts power, a Revision 6 power control board with a metal circular power connector that passes these voltages to the backplane, and heavy bus wires hand wired in to the pins B30 and C28 for carrying the +/- 6.5 volt current. Finally, the fifth regulator is a normal overhead part supplying +32 volts to the board, and requires several volts of overhead. The nominal input voltage for this supply to the board is between 35 and 36 volts.

BOARD JUMPERING

Fig. 3 shows an enlargement of the jumpers that need configuring on the board. The parts layout of the preamp and input offset circuitry is shown on the left where the top channel jumpers for channel A are shown configuring the preamp for AC coupling. The lower channel B is shown configured for DC coupled operation. For ease of setup the default jumpers are put in the AC coupled mode.

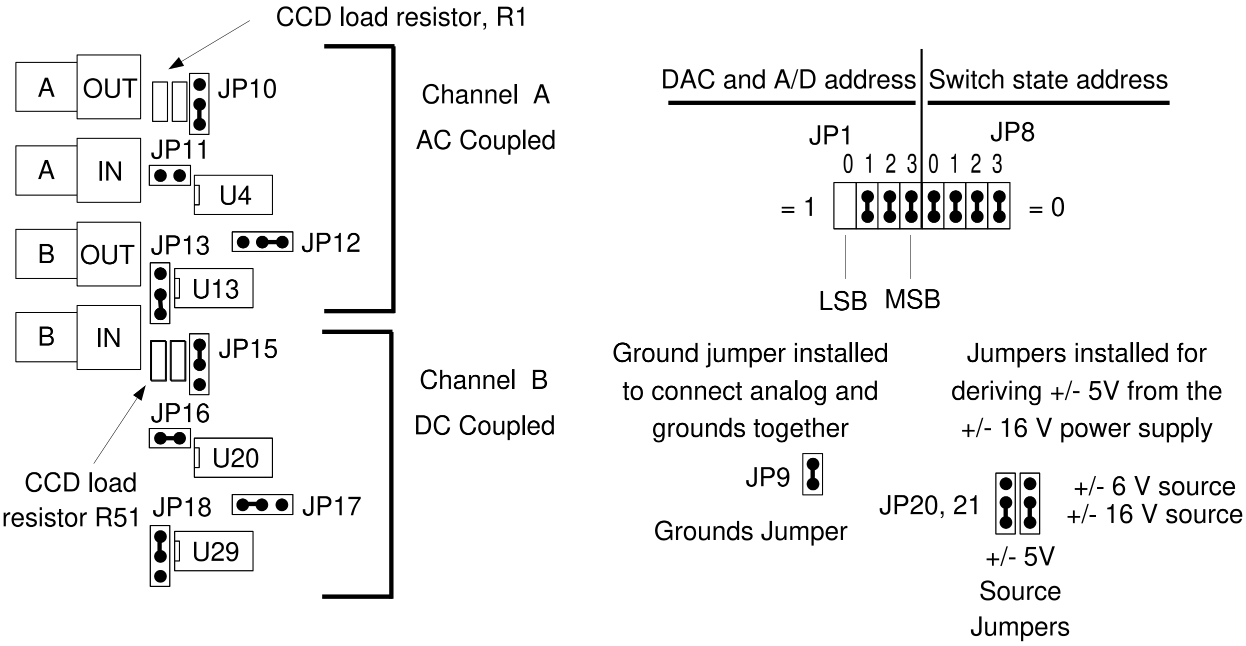

Fig. 3: Layout of preamp jumpers, input connectors and address jumpers

The ground jumper JP9 that is used to connect the analog and digital grounds planes on the board is shown in the figure. Lower readout noise has been found in prototype systems with the jumper installed, and on many boards this jumper is not installed but rather a wire is soldered in place of R92 right next to it. The user may cut the wire in R92 at will to break the connection between digital and analog ground planes if desired, and install a jumper header in JP9 to easily switch back and forth to determine the minimum noise configuration. The jumpers JP20 and JP21 select between obtaining the power for the +/- 5 volts regulated supplies from either +/-16.5 volts (jumpers on bottom) or from +/-6.5 volts (jumpers on top).

The board addressing jumpers JP1 to JP8 determine the addresses of the DACs, A/D converters and timing switches. The four jumpers on the left side JP1 to JP4 in the schematic, labelled DAC-A/D 0 to 3 on the silk screen layer on the board, determine the board address for reading the contents of the two A/D converters and for setting the value of the DACs. An installed jumper will be read as a zero, and an uninstalled jumper will be read as a one. The four jumpers set the address of the four most significant bits of the five addressing bits allowed in a system, with the least significant bit selecting the A (bit D0 = 0) or B (bit D0 = 1) channel. A maximum of sixteen video processing boards may be installed in a system. As discussed in the timing board user's manual, the A/D counts may be read either by the DSP reading from the RDAD memory mapped locations Y:$FFA0 to $FFBF. Alternately, the SXMIT command may be used to read a several A/Ds, possibly on several different boards, and transmit them as a series to the host computer, bypassing the timing board DSP entirely, as described in the timing board user's manual. The example below describes several different jumper settings and the DSP instructions required to read from a single video processor board.

JP1	JP2	JP3	JP4	DSP read	SXMIT	Comment
ON	ON	ON	ON	Y:$FFA0	$00F000	Only read one A/D from board 0
ON	ON	ON	ON	Y:$FFA0 and FFA1	$00F020	Read both A/Ds from board 0
OFF	ON	ON	ON	Y:$FFA2 and FFA3	$00F062	Read both A/Ds from board 1
ON	ON	OFF	ON	Y:$FFA8 and FFA9	$00F128	Read both A/Ds from board 4
OFF	OFF	OFF	OFF	Y:$FFBE and FFBF	$00F3FE	Read both A/Ds from board 15

And several examples for more than one A/D board:

JP1	JP2	JP3	JP4	DSP read	SXMIT	Comment
ON	ON	ON	ON	Y:$FFA0 to FFA3	$00F060	Read four A/Ds, boards 0 and 1
OFF	ON	ON	ON			
ON	OFF	ON	ON	Y:$FFA4 to FFA7	$00F0E4	Read four A/Ds, boards 2 and 3
OFF	OFF	ON	ON			

The jumper JP1 to JP4 also select the board address when the timing board writes to the DACs. The DAC and A/D board addresses are always the same, and there is one set of DACs per video board addressed from one jumper setting, allowing for a maximum of 16 video processor boards per system. The most significant bits D20 to D24 of the serial word written out over the backplane pins TIM-A-STD match the jumpers JP1 to JP4 to select the video processor board to be written to, and the bits D14-D17 select which of the four DACs on a board and which of each of its internal four DAC addresses is addressed, following Table 3 above. Bits D18 and D19 must be high to select a video processing board, while if they are not both high a clock driver DAC is addressed.

The four jumpers on the right side JP5 to JP8 in the schematic, labelled switch 0 to 3 on the silk screen layer, determine the address that the fast timing analog switches will respond to. Generally all the video boards in a system are have the same timing jumpers and have the same timing, though 16 timing addresses are provided. The supplied DSP code always sets the video board timing address to zero, and all four jumpers are installed.

Revision History -

Rev. 3B, dated 7/3/97 - includes a patched 51 pf capacitor on the input for noise filtering.