CTS®

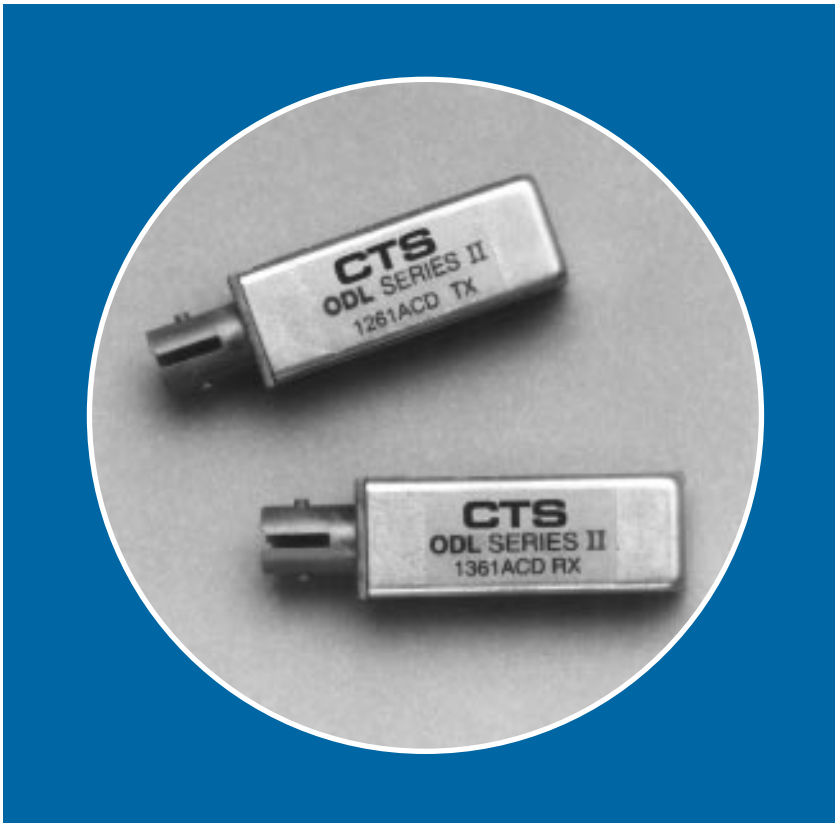
ODL® 70 Series II Lightwave Data Link

Technical Data

ODL® 70 Series II Lightwave Data Link

Features

- ac-coupled/burst-mode capabilities
- Positive ECL-compatible (PECL) signal levels
- 875 nm short wavelength or 1300 nm long-wavelength available
- High-strength, 16-pin plastic package with *ST*® Receptacles
- Wide dynamic range
- EMI-shielded
- Low-cost, conductive, plastic housing



The *ODL* 70 Series II Data Link can accommodate both burst-mode and ac-coupled applications.

Applications

- Telecommunications
  - — Network control and timing
  - — Link between PBX modules
  - — Local loops
- Data communications
  - — Locals area networks (LANs)
  - — Point-to-point
  - — Channel extenders
- Secure communications
  - — Banking
  - — Military
  - — Channel extenders

Benefits

- Economical, corrosion-resistant package
- High-reliability modules incorporate single IC design
- Compatible with various fiber sizes
- Allows single-voltage board design using 5 V power supply

Description

The ODL 70 Series II Lightwave Data Link is a high-performance transmitter and receiver pair designed to operate efficiently over the entire data rate range of dc to 70 Mbits/s at a typical distance of up to 3 km. Both devices require a single 5 V power supply, and each employs a single IC to perform data-handling functions.

Operating at an 870 nm (or 1300 nm) wavelength, the transmitter and receiver modules can handle positive ECL logic levels.

ECL to TTL

The standard ODL 70 Transmitter (1261ACD) is compatible with positive ECL logic levels. For TTL-level applications, however, the ECL transmitter can be replaced by its TTL counterpart, the 1261AAC Transmitter. Conversely, the receiver can be converted from raised-ECL to TTL by incorporating a Line Driver.

Burst Mode/ac Coupling

The 1361ACD Receiver is a versatile, reconfigurable device specially designed to accommodate varying duty cycles. The module, for example, can be set up as a burst-mode receiver for low duty-cycle applications between dc and 50 Mbits/s.

For higher speeds from 10 Mbits/s to 70 Mbits/s and for greater sensitivity, the receiver can also be configured to deliver optimum performance in an ac-coupled mode.

Long-Wavelength Options (1361 BCB)

At data rates under 32 Mbits/s, the low-cost Series II is also available with an option for long-wavelength operation. In this configuration, the recommended transmitter is the 1261BCE (see ODL 125 Data Sheet). The receiver is a custom part combining an InGaAs photodetector with circuitry of the 1361ACD to achieve performance specifications similar to those shown in this data sheet. The long-wavelength receiver is configurable for burst-mode or ac-coupled applications and operates at positive ECL logic levels as well.

Lightweight, Compact Package

The transmitter and receiver are offered in identical, high-strength, plastic packages with a standard 16-pin DIP footprint. The *ST* Connector port and housing frame are made of high-strength engineering plastic. The plastic offers corrosion resistance while maintaining high heat resistance (>200 °C) and has UL V-O flame-retardancy properties. Metal covers are used to provide receiver shielding and LED heat-sinking for high-reliability applications.

The *ODL* 70 Series II Data Link is designed for 62.5/125 µm optical fiber but is also compatible with other multimode fiber sizes. (See Table 1.)

Optional Data Scrambler (Short Wavelength Only)

The *ODL* 70 transmitter contains an optional-use seven-stage data scrambler. The pin-selectable scrambler enriches the data stream and provides an average duty cycle of 50% for the transmitted data.

The scrambler is enabled by tying pin 4, SCR SEL, to V_{EE}, the negative supply rail. When pin 4 is tied to Vcc, the positive supply rail, the scrambler is disabled.

When using the scrambler feature, it is necessary to apply a clock signal to pin 2. Descrambling the data at the receiver end requires the use of a Clock Recovery Circuit (CRC).

If the scrambler feature is not being utilized, pin 2 may be left unconnected.

Description (continued)

Table 1. ODL Series II Lightwave Data Link Fiber Compatibility

All values are typical and are referenced to standard Lightguide Multimode Fiber (62.5/126 μm).

Fiber Size (μm)*	Transmitter Launch Power Change (dB)	Receiver Sensitivity Change (dB)†
50/125	–2.5	0
62.5/125	0	0
85/125	+1.8	0
100/140	+3.0	0

* Inner-core/outer-core diameters.

† Does not include the additional dispersion due to differences in fiber-core sizes.

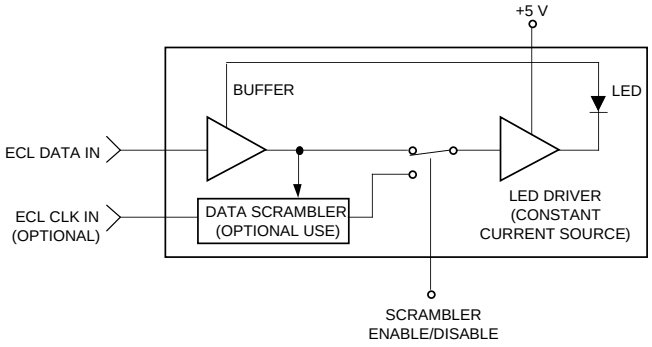
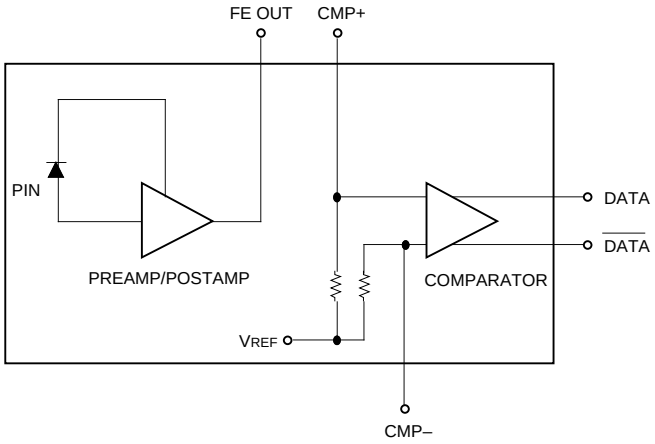
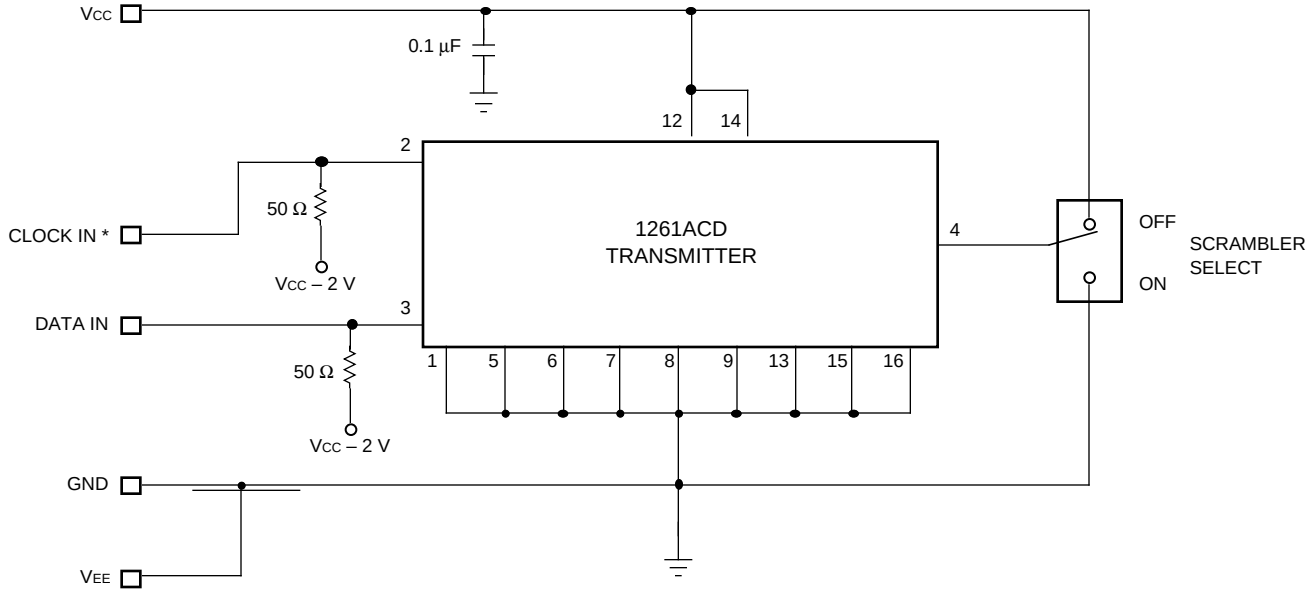


Figure 1. *ODL* 70 Series II ECL Transmitter (1261ACD) Block Diagram



Note: All components shown are integrated on a single IC (with the exception of the PIN detector).

Figure 2. *ODL* 70 Series II Burst Mode/ac-Coupled Receiver (1361ACD) Block Diagram (Long-wavelength version (1361BCB) has the same pinout.)

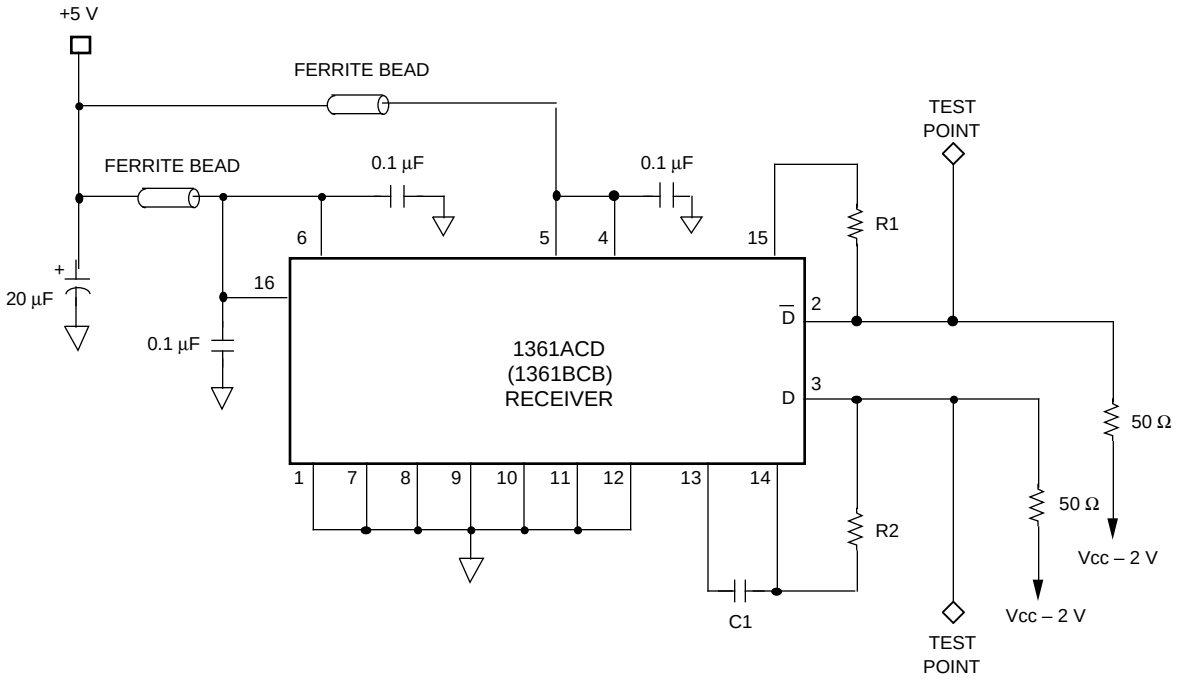


POSITIVE = V_{EE} = GND.

* Optional — used only with scrambler.

Figure 3. Test Circuit for the 1261 ACD ECL Transmitter

Description (continued)



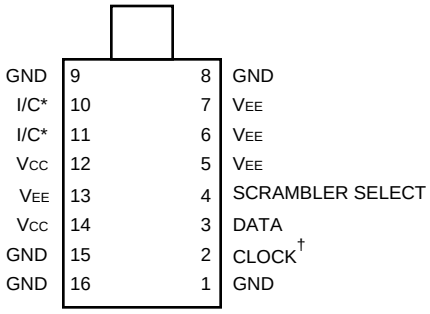
Configuration	C1	R1 and R2
Burst Mode	100 pF	4 kΩ
ac Coupled	0.1 µF	Not Used

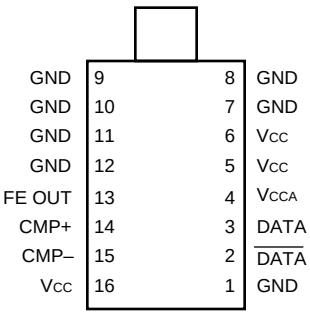
Note: C1 should be a ceramic capacitor and placed as close to pins 13 and 14 as possible.

Figure 4. Test Circuit for the 1361ACD and 1361BCB Reconfigurable Receiver

Pin Information

Top view





* Internal connection; must be left as an open circuit.
† Use only with scrambler.

Figure 5. Transmitter Pin Diagram

Figure 6. Receiver Pin Diagram

Printed-Wiring Board Layout

As with any sensitive or high-speed electronic component, to obtain optimum performance from the device, careful attention must be given to the printed-wiring board. Board layout is crucial for achieving rated performance. The routing of sensitive input traces relative to other components and signal lines must be considered in great detail. Data lines must be of controlled impedance and properly terminated to minimize reflections that might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering.

Printed-Wiring Board

As a minimum, a double-sided printed-wiring board having a large ground plane on the component side, directly beneath the devices, should be utilized. In applications where a large number of other devices are included on the circuit card, a multilayer circuit board is preferred. This allows for the separation of power and ground connections, and provides isolation for sensitive traces from high-level signals that might couple to the sensitive inputs.

In either case, the ideal approach is to have the ground plane as close to the devices as possible and to cover as much of the printed-wiring board as possible. For maximum EMI shielding, the receiver's and transmitter's conductive housing should be connected to the PWB using two #1 self-tapping screws into the holes provided.

Power Supply Filtering

Noise that couples into the transmitter/receiver pair through the power supply pins can also degrade device performance. In the Receiver, pins 6 and 16 provide the power supply bias to the very sensitive, front-end photodetector and amplifier circuits; pins 4 and 5 provide bias to the higher-level comparator (decision) circuit.

To minimize coupled power supply noise, the power supply circuit filter shown in Figure 4 is recommended. The 0.1 μF capacitors should be high-quality ceramic devices rated for RF applications. Place the capacitors as close as physically possible to the V_{CC} pins. Surface-mount capacitors mounted adjacent to the power supply pins is the ideal setup.

Layout Considerations

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. It is designed to detect and amplify signal levels that are only nanoamperes in amplitude. Any unwanted signals which couple into the receiver circuitry will cause a decrease in the receiver's sensitivity and may also degrade the performance of the receiver's signal detect indicators.

To minimize the coupling of unwanted noise into the receiver, transmitter input traces and other traces carrying high-level or high-frequency signals should be routed as far away as possible from the receiver pins. If wide separation is not possible, then the receiver pins and traces connected to them should be shielded by placing a ground trace between the receiver's pins and connecting traces and other high-level signal paths.

When laying out the printed-wiring board for the devices, note that the plastic housing is conductive. Avoid placing topside metal or vias that are not at ground potential in the areas beneath the housing standoffs or beneath the areas where the metal shield is soldered to the package (see Outline Drawing). The preferred PWB layout for these devices is to employ a ground plane on the component side of the board, directly under the transmitter and receiver.

Data Lines

The signals on the data lines typically have rise and fall times on the order of 1 ns to 2 ns. If the data lines are not properly handled, the fast transitions cause EMI problems as well as electrical reflections and excessive ringing, which degrade the performance of the transmitter/receiver pair. When laying out the traces for the data lines, follow high-speed ECL design guidelines as described in the *Motorola MECL System Design Handbook*.

- All high-speed output lines must use controlled-impedance traces and have the termination impedance match the trace impedance. Controlled-impedance interruptions must be avoided (i.e., 90° bends, etc.), and paired lines (i.e., DATA and $\overline{\text{DATA}}$ should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination resistor.
- Data output lines should be as short and straight as possible and should be isolated from noise sources to prevent noise from feeding back into the receiver.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–40	100	°C
Lead Soldering Temperature/Time	—	—	240/10	°C/s
Transmitter Supply Voltage	$V_{CC} – V_{EE}$	0	6.0	V
Transmitter Input Voltage	V_{IH}	0	V_{CC}	V
Receiver Supply Voltage	V_{CC}	0	6.0	V
Receiver Output Current	I_{OS}	—	50	mA

Electrical/Optical Characteristics

Table 2. Transmitter Section[1] (See Figure 3.)

$V_{CC} – V_{EE}$ = 4.75 V to 5.25 V; operating case temperature: 0 °C to 70 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Data Rate	BR	dc	—	70	Mbits/s
Input Voltage:[2]					
Low	V_{IL}	–1.181	—	–1.149	V
High	V_{IH}	–1.165	—	–0.88	V
Power Supply Current Drain	I_{CC}	—	115	160	
Peak Optical Power[3]	P_{OH}	–16 (25)	–13 (50)	—	dBm (μW)
Static Extinction Ratio (P_{OH}/P_{OL})[4]	ER	100 (20)	>200 (>23)	—	(dB)
Output Optical Rise Time[5,6]	t_R	—	5	7	ns
Output Optical Fall Time[5,6]	t_F	—	5	7	ns
Propagation Delay	t_{PLH}	—	11	17	ns
	t_{PHL}	—	11	17	ns
Pulse Width Distortion[6]	PWD	—	2	4	ns
Center Wavelength	λ	850	875	900	nm
Spectral Width (FWHM)	Δλ		50	70	nm

1. All specification values (minimum/maximum) include temperature and supply voltage variations. Typical values are at $V_{CC} – V_{EE}$ = 5 V and 25 °C. Input voltage and current values are dc specifications. All other values are determined at 70 Mbits/s with a $2^7 – 1$ pseudorandom word length and NRZ coding except where noted.
2. Note that the technology used is ECL compatible CMOS. As with all CMOS devices, the data and the clock inputs (pins 3 and 2, respectively) must **not** be applied before Vcc. In addition, any input must **not** exceed Vcc or be less than V_{EE}. This recommendation is intended to minimize the potential of latch-up problems. These modules have ESD-protection circuitry. Input voltage is measured from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
3. Steady-state, beginning-of-life peak power coupled into 0.275 NA (determined by the Far-Field Radiation Pattern Measurement described in EIA test procedure RS-455-47), 62.5/125 μm connectorized fiber. Peak optical power is defined as average power plus 3 dB.
4. POL is defined as the peak optical power at logic-low.
5. Rise and fall times are for 10% and 90% transition times. A square wave (1010 . . .) is used as the data stream input.
6. This is specified with a condition that the input data is **not** distorted and the scrambler is disabled. Our test signal input is 800 mV peak-to-peak, centered at V_{CC} – 1.32.

Electrical/Optical Characteristics (continued)

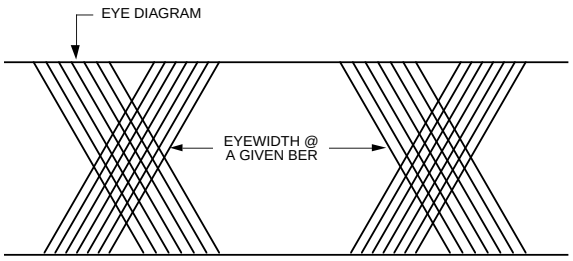
Table 3. Receiver Section[1] Short Wavelength (See Figure 4.)

V_{CC} – V_{EE} = 4.75 V to 5.25 V; operating case temperature: 0 °C to 70 °C.

Parameter	Symbol	Burst Mode[2]			ac Coupled[3]			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current Drain	Icc	—	75	110	—	75	110	mA
Optical Wavelength for Rated Sensitivity	ƛ	825	—	900	825	—	900	nm
Output Voltage:								
Low	V_{OL}	–1.82	—	–1.61	–1.82	—	–1.61	V
High	V_{CH}	–1.04	—	–0.88	–1.04	—	–0.88	V
Output Rise Time[4]	t_R	—	1.3	3.5	—	1.3	3.5	ns
Output Fall Time[4]	t_F	—	1.3	3.5	—	1.3	3.5	ns
Data Rate	BR	dc	—	50	10	—	70	Mbits/s
Peak Optical Sensitivity[5] (@ 10-9 BER)	SEN	—	–27	–24	—	–32	–29	Mbits/s
Average Optical Sensitivity	ASEN	—	–30	–27	—	–35	–32	dBm
Maximum Optical Input Power (Peak) @ 10^{-9} BER[6]	$P_{IN\ MAX}$	—	—	–11	—	—	–11	dBm
Eyewidth[7] @ 10^{-9} BER	EW	13	16	20	8	11	14.3	ns
Pulse-Width Distortion[8]	PWD	—	2.6	5.0	NA	NA	NA	ns

1. All specification values (minimum/maximum) include temperature and supply voltage variations. Output voltage values are dc specifications. Typical characteristics are at 25 °C and nominal voltage.
2. Output voltage measured from V_{CC} with a 50 Ω load to (V_{CC} – 2). All dynamic tests are performed at 50 Mbits/s with a 2^7 – 1 pseudorandom word length with a 50% duty cycle and NRZ coding, except where noted, by using standard raised-ECL terminations on both data and not data outputs (50 Ω to V_{CC} – 2).
3. Output voltage measured from Vcc with a 50 Ω load to (V_{CC} – 2). All dynamic tests are performed at 50 Mbits/s with a 2^7 – 1 pseudorandom word length and NRZ coding, except where noted, by using standard raised-ECL terminations on both data and not data outputs (50 Ω to V_{CC} – 2).
4. Rise and fall times are measured from 10% and 90% transition times with an average optical power input of –23 dBm. A square wave (1010 . . .) is used as the data stream input.
5. Peak optical receiver sensitivity is defined as the average optical sensitivity plus 3 dB.
6. This device has operated satisfactorily with peak optical input levels as high as –10 dBm.
7. Determined with an average optical power input of –27 dBm (50 Mbits/s burst mode) or –28 dBm (50 Mbits/s ac coupled).
8. Input pattern is a repetitive 32-bit word containing a 1 with 31 zeros or the complement of this pattern. The input optical pulse should have <0.25 ns pulse-width distortion at the 50% point and should have a –12 dBm peak optical power. The output, using proper terminations (see note 3), should be measured at the 50% point.

Figure 7. Description of Eyewidth



Electrical/Optical Characteristics (continued)

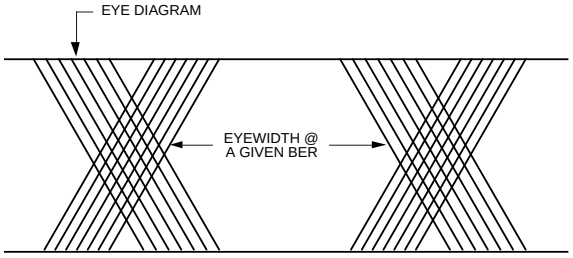
Table 4. Receiver Section,[1] Long Wavelength (See Figure 4.)

V_{CC} – V_{EE} = 4.75 V to 5.25 V; operating case temperature: 0 °C to 70 °C.

Parameter	Symbol	Burst Mode[2]			ac Coupled[3]			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current Drain	Icc	—	75	110	—	75	110	mA
Optical Wavelength for Rated Sensitivity	λ	1270	1312	1380	1270	1312	1380	nm
Output Voltage:								
Low	V_{OL}	–1.82	—	–1.61	–1.82	—	–1.61	V
High	V_{CH}	–1.04	—	–0.88	–1.04	—	–0.88	V
Output Rise Time[4]	t_R	—	—	2.5	—	—	2.5	ns
Output Fall Time[4]	t_F	—	—	2.5	—	—	2.5	ns
Data Rate	BR	dc	—	32	10	—	32	Mbits/s
Peak Optical Sensitivity[5] (@ 10-9 BER)	SEN	—	—	–22.5	—	—	–27.5	Mbits/s
Average Optical Sensitivity	ASEN	—	—	–25.5	—	—	–30.5	dBm
Maximum Optical Input Power (Peak) @ 10^{-6} BER[6]	$P_{IN\ MAX}$	—	—	–10	—	—	–10	dBm
Eyewidth[7] @ 10^{-9} BER[6]	EW	—	—	—	24.5	—	29.6	ns
Pulse-Width Distortion[8]	PWD	—	2.6	5.0	NA	NA	NA	ns

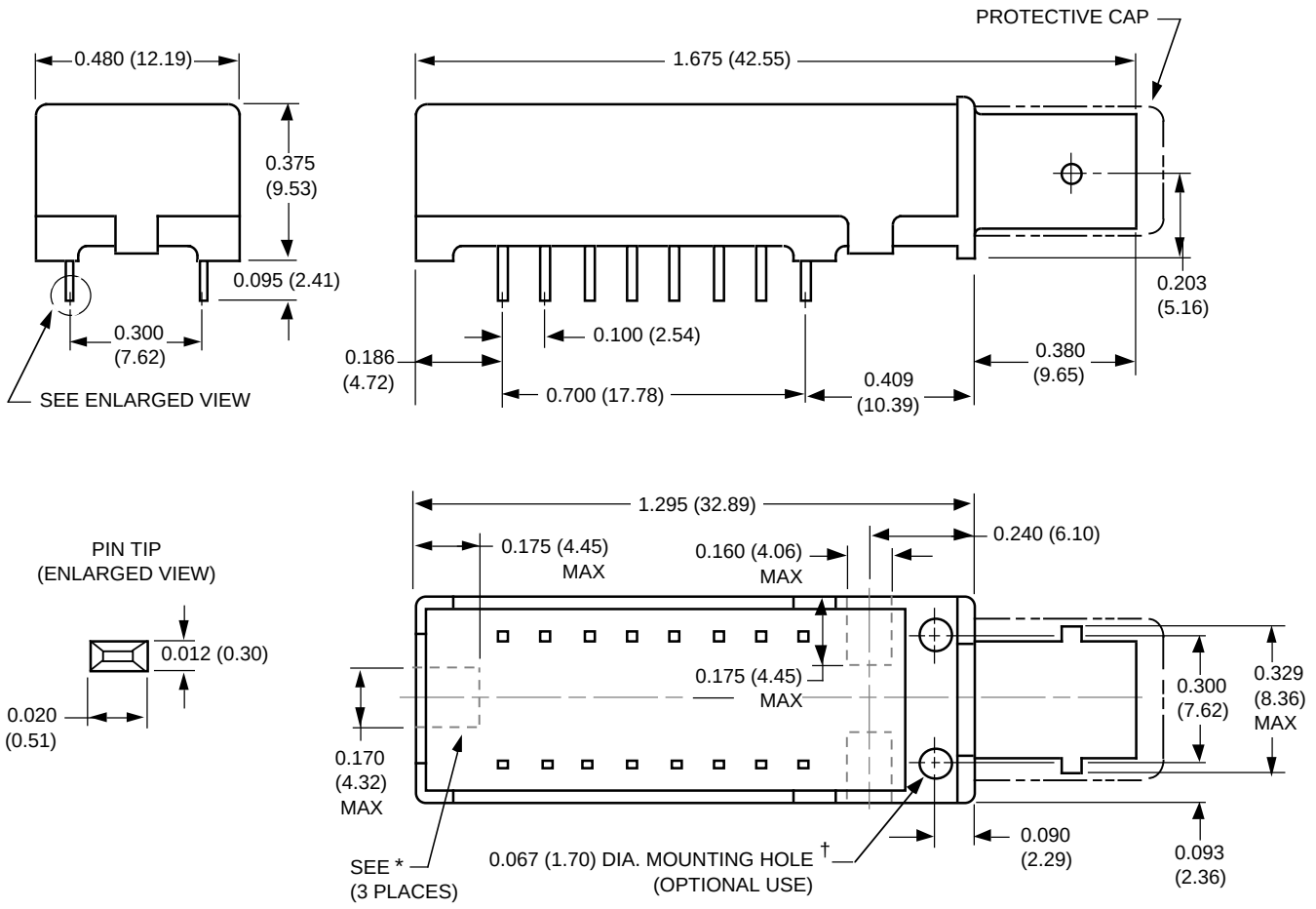
1. All specification values (minimum/maximum) include temperature and supply voltage variations. Output voltage values are dc specifications. Typical characteristics are at 25 °C and nominal voltage.
2. Output voltage measured from V_{CC} with a 50 Ω load to (V_{CC} – 2). All dynamic tests are performed at 32 Mbits/s with a 2^7 – 1 pseudorandom word length with a 50% duty cycle and NRZ coding, except where noted, by using standard raised-ECL terminations on both data and not data outputs (50 Ω to V_{CC} – 2).
3. Output voltage measured from Vcc with a 50 Ω load to (V_{CC} – 2). All dynamic tests are performed at 32 Mbits/s with a 2^7 – 1 pseudorandom word length and NRZ coding, except where noted, by using standard raised-ECL terminations on both data and not data outputs (50 Ω to V_{CC} – 2).
4. Rise and fall times are measured from 10% and 90% transition times with an average optical power input of –23 dBm. A square wave (1010 . . .) is used as the data stream input.
5. Peak optical receiver sensitivity is defined as the average optical sensitivity plus 3 dB.
6. This device has operated satisfactorily with peak optical input levels as high as –10 dBm.
7. Determined with an average optical power input of –27 dBm.
8. Input pattern is a repetitive 32-bit word containing a 1 with 31 zeros or the complement of this pattern. The input optical pulse should have <0.25 ns pulse-width distortion at the 50% point and should have a –12 dBm peak optical power. The output, using proper terminations (see note 3), should be measured at the 50% point.

Figure 7. Description of Eyewidth



Outline Diagram (Transmitter and Receiver)

Dimensions (typical) are in inches and (millimeters).



* Do not place signal or power supply metal within **outlined areas around solder tabs.** Metal shield and plastic housing are at ground potential.

† Use a #1 self-tapping screw. Insert screw before soldering module on PWB. Maximum length = 0.3 in. + circuit board thickness.

Ordering Information

Table 5. Ordering Information

Device	Part Number
ODL 70 Series II ECL Transmitter	1261ACD
ODL 70 Series II Reconfigurable Receiver	1361ACD
ODL Long-Wavelength Receiver (<32 Mbits/s)	1361BCB

Notes

Order From

Or for additional information, contact your local CTS Distributor, Agent, Sales Representative or in:

U.S.A., EUROPE, ASIA PACIFIC:

CTS Microelectronics, 1201 Cumberland Avenue, W. Lafayette, Indiana 47906
Phone 317-463-2565, FAX 317-497-5399

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CTS Corporation, Japan Sales Office, Mori Building No. 32, 4F, 4-30, 3 Chome Shibakoen, Minato-ku Tokyo 105, Japan
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