CTS®

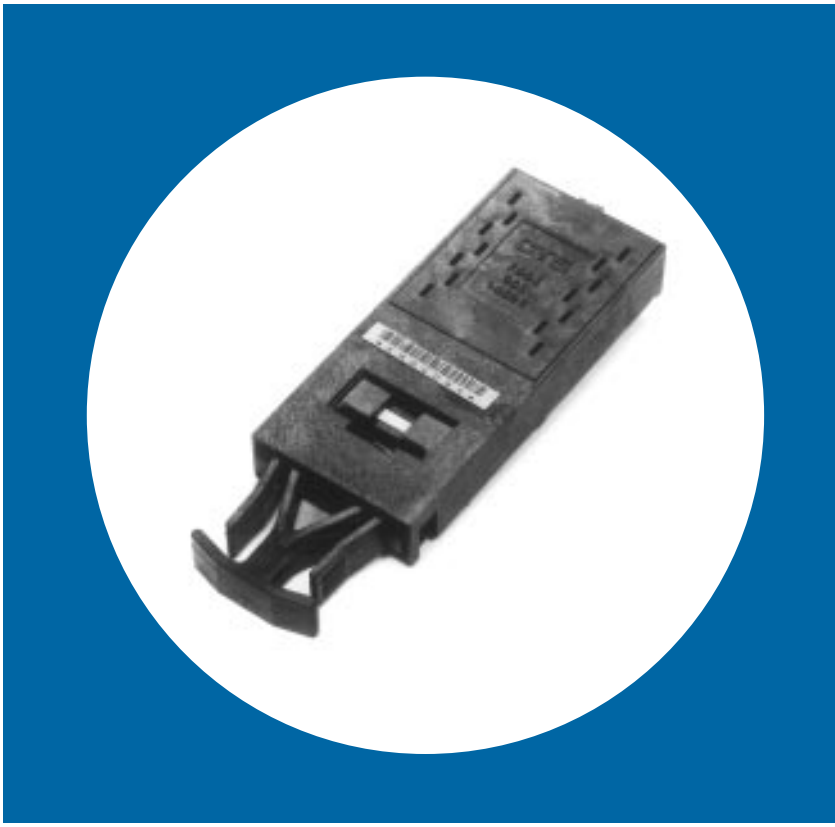
1402C *ODL*® FDDI Transceiver

Technical Data

1402C *ODL*® FDDI Transceiver

Features

- FDDI (fiber distributed data interface)-compliant specifications
- Conforms to industry-standard 22-pin configuration
- Low power dissipation
- Differential signal-detect indicator
- Single +5 V power supply
- Field keyable
- Improved transmitter end-of-life (EOL) performance
- Low EMI/RFI emissions and susceptibility
- Low ESD susceptibility
- Compatible with 10KH and 100KH ECL logic
- Compatible with typical wave soldering and aqueous cleaning processes (with process plug)



The 1402C *ODL* FDDI Transceiver package features a 2x11-pin footprint.

Applications

- Data communications
  - — Local area networks (FDDI)
  - — Point-to-point communications
  - — Channel extenders
- Secure communications
  - — Banking
  - — Military

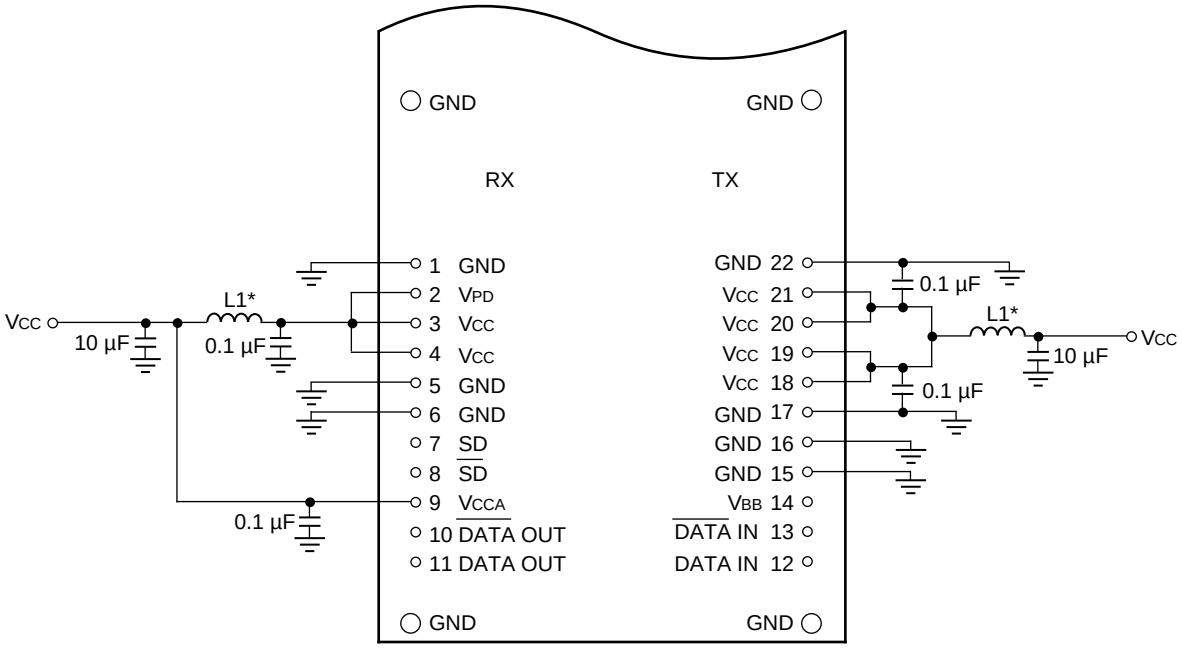
Description

The 1402C *ODL* FDDI Transceiver is a high-performance, cost-effective link that meets the American National Standard Institute's specifications for FDDI-compliant fiber-optic components. The transceiver operates from 10 Mbits/s to 125 Mbits/s (NRZ) at a typical distance of 3 km. Available with an industry-standard pin configuration, the transceiver package mates directly to the FDDI media interface connector (MIC). The package also features the FDDI multi-source field-installable key. The customer can configure the receptacle to meet any of the four FDDI keys.

All *ODL* FDDI Transceivers meet or exceed the specifications defined in the FDDI PMD document.

Pin Information

Top view.



* L1 — Ferrite bead; Fair-Rite Products Corp., Part Number 2743002111 or equivalent.

Figure 1. Pin Diagram

Printed-Wiring Board Layout

As with any sensitive or high-speed electronic component, to obtain optimum performance from the FDDI transceiver, careful attention must be given to the printed-wiring board. The routing of sensitive input traces relative to other components and signal lines must be considered in great detail. Data lines must be of controlled impedance and properly terminated to minimize reflections that might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering.

Printed-Wiring Board

As a minimum, a double-sided printed-wiring board having a large ground plane on the component side should be utilized. In applications where a large number of other devices are included on the circuit card, a multilayer circuit board is preferred. This allows for the separation of power and ground connections, and provides isolation for sensitive traces from high-level signals that might couple to the sensitive inputs.

In either case, the ideal approach is to have the ground plane as close to the transceiver as possible and to cover as much of the printed-wiring board as possible.

Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth, transimpedance amplifier. The amplifier detects and amplifies signal levels that are only nanoamperes in amplitude. Any unwanted signals that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal-detect indicators.

To minimize the coupling of unwanted noise into the receiver, route transmitter-input traces and other traces carrying high-level signals as far away as possible from the receiver pins. If wide separation of the receiver pins from other high-level signal lines is not possible, the receiver pins and traces connected to them should be shielded by placing a ground trace between the receiver's pins and connecting traces and other high-level signal paths.

Printed-Wiring Board Layout

(continued)

Power Supply Filtering

Noise that couples into the transceiver through the power supply pins can also degrade device performance. Figure 1 shows the recommended power supply filtering for both the transmitter and receiver power supply pins. The 0.1 µF capacitors should be high-quality ceramic devices rated for RF applications. Place the capacitors as close as physically possible to the V_{CC} pins. The ideal situation is surface-mount capacitors mounted up against the power supply pins.

In some instances, especially on double-sided circuit boards in noisy environments, it may be necessary to provide separate filtering for the V_{PD} bias pin on the receiver. Do this by placing a separate 0.1 µF capacitor from pin 2 to ground, and connecting pin 2 to V_{CC} through a separate ferrite bead.

Data Lines

The signals on the data lines typically have rise and fall times on the order of 1 ns to 2 ns. If the data lines are not properly handled, the fast transitions cause EMI problems as well as electrical reflections and excessive ringing, which degrade the performance of the transceiver. When laying out the traces for the data lines, follow high-speed ECL design guidelines as described in the *Motorola MECL System Design Handbook*.

- All high-speed output lines must use controlled-impedance traces and have the termination impedance match the trace impedance. Controlled-impedance interruptions must be avoided (i.e., 90° bends, etc.), and paired lines (i.e., DATA and $\overline{\text{DATA}}$) should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination resistor.
- Data and signal-detect output lines should be as short and straight as possible and should be isolated from noise sources (and each other) to prevent noise from feeding back into the receiver.

Test Qualifications

The 1402C Transceiver has successfully passed the following qualifications.

Test	Conditions	Sample Size	Failure Criteria
Physical Dimensions	JESD22-B100	90	Dimensional
External Visual	JESD22-B101	90	Visual
Impact Shock	JESD22-B104 Condition A	24	Electrical/optical
Variable Frequency Vibration	JESD22-B103	24	Electrical/optical
Solderability	JESD22-B102	12	Visual
Lead Integrity	JESD22-B105	10	Visual
Temperature Cycle (pre condition)	JESD22-A104 (-40°C to + 100°C for 5 cycles)	90	Electrical/optical
Temperature Cycle	JESD22-A104 (0°C to + 100°C, 1000 cycles)	30	Electrical/optical
High Temperature, Humidity with Bias	JESD22-A101 (500 hours)	30	Electrical/optical
High Temperature Operating Bias	JESD22-A108 (1000 hours)	30	Electrical/optical
Connector Repeatability	500 cycles	5	Optical

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–40	100	°C
Lead Soldering Temperature/Time[1]	—	—	240/10	°C/s
Supply Voltage[2]	V_{CC}	0	6.5	V
Output Current[3]	I_O	—	50	mA
Input Voltage[4]	V_I	0	V_{CC} + 0.5	V
Differential Input Voltage	—	—	2.0	V

1. Applies to electrical pins only.
2. Measured from ground to V_{CC}.
3. From DATA and $\overline{DATA}$ outputs of receiver.
4. Voltage at DATA or $\overline{DATA}$ input terminals of transmitter measured from V_{CC}.

Handling Precautions

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the transceiver, take proper precautions to avoid exposure to ESD.

CTS employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The 1402C was characterized to an HBM ESD threshold of ±1500 V using these parameters.

Transceiver Processing

When the process plug is placed in the transceiver, it is able to withstand normal wave soldering and aqueous cleaning. The transceiver is not hermetically sealed, so it cannot be immersed in any solutions. The transceiver case and process plug deformation temperature is 150 °C. The transceiver pins can be wave soldered at 240 °C for up to 10 s.

The process plug should only be used once. After removing the process plug from the transceiver, it must not be used as a process plug again; however, if it has not been contaminated, it can be used as a dust cover. See Ordering Information to obtain additional process plugs.

Electrical Characteristics

Table 1. Transmitter Section

The transceiver is FDDI-compliant over the following conditions: V_{CC} – V_{EE} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary inputs.[1, 2]

Parameter	Symbol	Min[2]	Typ[3]	Max[2]	Unit
Input Data Voltage:[4]					
Low	V_{IL}	–1.810	—	–1.475	V
High	V_{IH}	–1.165	—	–0.880	V
Input Current:					
Low[5]	I_{IL}	0.5	–0.025	—	µA
High[6]	I_{IH}	—	0.045	2.00	µA
Reference Voltage[7]	V_{BB}	–1.390	–1.310	–1.20	V
Power Supply Current[9]	L_{CC}	–	100	130	mA
Data Rate (NRZ encoding)	DR	0	—	125	Mbits/s
Average Optical Power (BOL)[10,11]	P_O	12.6 (–19.0)	23.4(–16.3)	39.8(–14.0)	µW(dBm)
Disable Power (input low)[12]	P_{OL}	—	<0.001(<–60)	0.03(–45.0)	µW(dBm)
Dynamic Extinction Ratio[8,13]	EXT_S	—	2.0	10.0	%
Output Rise Time[8,14,18,19]	t_R	0.6	2.3	3.5	ns
Output Fall Time[8,14,18,19]	t_F	0.6	2.5	3.5	ns
Optical Wavelength (center)[19]	λ_C	1270	1315	1380	nm
Power Dissipation[15]	P_{DISS}	—	0.5	0.72	W
Data-dependent Jitter[16]	DDJ	—	0.2	0.6	ns (p-p)
Random Jitter[17]	RJ	—	0.3	0.7	ns (p-p)
Duty-cycle Distortion[17]	DCD	—	0.1	0.6	ns (p-p)

1. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-endedly.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges.
3. Typical values are measured at room temperature.
4. Measured from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
5. Measured at V_{IL} = V_{IL}, min.
6. Measured at V_{IH} = V_{IH}, Max.
7. Measured from V_{CC}.
8. Measured with the FDDI specified, halt-line-state input (12.5 MHz square wave).
9. No load on VBB.
10. Values given are at beginning of life (BOL) and from 0°C to 70°C ambient. A reduction in optical power of 1.0 dB should be allowed over 100,000 hours lifetime.
11. Measured average power coupled into 0.275 NA, 62.5/125 µm fiber.
12. The optical output power with a logic-low at the input.
13. Ratio of the optical power in the logic-low state to the optical power in the logic-high state.
14. Between 10% and 90% points.
15. Maximum value specified with a 5.5 V power voltage.
16. Measured output jitter by using an input of 125 Mbits/s worst-case data pattern specified in FDDI PMD Appendix A, having negligible DDJ.
17. Measured with an input of 125 Mbits/s 1010 pattern having neglibible DCD or random jitter.
18. The optical output pulse is contained within the optical pulse envelope as specified by ANSI X3T9.5 PMD, Figures 5.2 and 5.3. See Figure 2 of this data sheet.
19. The optical rise time, fall time, center wavelength, and spectral width fit within the boundaries outlined in ANSI X3T95 PMD, Figure 5.1. See Figure 3 of this data sheet.

Electrical Characteristics (continued)

Table 2. Receiver Section

See notes, page 7.

V_{CC} = 4.5 V to 5.5 V; T_A = 0 °C to 70 °C; complementary outputs.[1, 2]

Parameter	Symbol	Min[2]	Typ[3]	Max[2]	Unit
Output Data Voltage:[4]					
Low	V_{OL}	–1.810	–1.70	–1.620	V
High	V_{OH}	–1.025	–0.95	–0.800	V
Receiver Current Drain:[5]	I_{CC}	—	100	140	mA
Data Rate (NRZ encoding)	DR	10	—	125	Mbits/s
Eyewidth[6]	EW	2.1	5.0	8.0	ns
Average Optical Sensitivity[7]	P_I	—	0.20(–37.0)	0.40(–34.0)	µW(dBm)
Average Maximum Input Power[8]	P_{MAX}	39.8(–14.0)	63.1(–12.0)	—	µW(dBm)
Optical Wavelength for Rated Sensitivity	ƛ	1270	–	1380	nm
Output Rise Time [9,10]	t_R	0.5	0.9	2.5	ns
Output Fall Time [9,10]	t_F	0.5	0.6	2.5	ns
Power Dissipation, V_{CC} [11]	P_{DISS}	—	0.5	0.77	W
Output Signal-detect Voltage: [4,12]					
Low	V_{FL}	–1.810	–1.70	–1.620	V
High	V_{FH}	–1.025	–0.95	–0.800	V
Signal-detect Assert Level (avg. power):					
Increasing Light Input [12]	S_{DAL}	–39.5	–35.5	–32.0	dBm
Signal-detect Deassert Level (avg. power):					
Decreasing Light Input [12]	S_{DDL}	–41.0	–37.3	–33.5	dBm
Signal Detect: Hysteresis[12]	HYS	1.5	1.8	—	dBm
Signal-detect Timing:					
Assert[13]	S_{DTA}	—	25	100	µs
Deassert[14]	S_{DTD}	—	40	350	µs
Data Output Timing:					
Assert[15]	D_{TA}	—	<1	15	µs
Deassert[16]	D_{TD}	12	50	—	µs
Duty-cycle Distortion[17]	DCD	—	0.1	0.4	ns (p-p)

Electrical Characteristics (continued)

Table 2. Receiver Section (continued)

1. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved by using either output individually.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges.
3. Typical values are measured at room temperature.
4. Measured from V_{CC} with a 50 Ω load to (V_{CCA} – 2.0 V).
5. With 50 Ω loads on DATA, $\overline{\text{DATA}}$, Signal Detect, and $\overline{\text{Signal Detect}}$ to (V_{CC} – 2.0 V).
6. During an 8 ns bit-period, eyewidth is the time span in which the bit error rate (BER) is less than 2.5×10^{-10}. Eyewidth is measured with a 125 Mbits/s optical input that uses the data pattern specified in Appendix A of the FDDI PMD. An average optical power of –32.5 dBm is used for the receiver. The input is coupled from a 0.275 NA, 62.5/125 μm fiber.
7. Average optical power coupled from a 0.275 NA, 62.5/125 μm fiber at 125 Mbits/s with a $2^7 – 1$ pseudorandom data pattern with a 50% duty cycle for a BER of 2.5×10^{-10}.
8. The maximum average input power corresponds to a minimum eyewidth of 2.5 ns at 2.5×10^{-10} BER.
9. Specified at a 125 Mbits/s data rate.
10. Between the 20% and 80% points with a 50 Ω load to (V_{CC} – 2.0 V).
11. With a +5.5 V power supply, 50% duty cycle, and logic outputs terminated in 50 Ω to (V_{CC} – 2.0 V).
12. Signal-detect output is logic 1 for light input levels above the indicated switching level and logic 0 for input levels below the indicated switching level. Whenever the signal detect is asserted, the BER of the data outputs is less than or equal to 0.01.
13. The value specified is the maximum time it takes the signal detect to assert after a step increase in the optical power into the receiver. Measured with the data pattern specified in Appendix A of the FDDI PMD.
14. The value specified is the maximum time it takes the signal detect to deassert after a step decrease in the optical power into the receiver. Measured with the data pattern specified in Appendix A of the FDDI PMD.
15. The value specified is the maximum time before the receiver data outputs reflect a BER of better than 0.01; measured starting after signal detect's assertion.
16. The value specified is the minimum time before the receiver data outputs reflect a no-light condition with a BER of 0.01 or worse; measured from the time the receiver begins receiving a no-light input.
17. Measured with an input 1010, 125 Mbits/s data pattern having negligible duty-cycle distortion.

Characteristic Curves

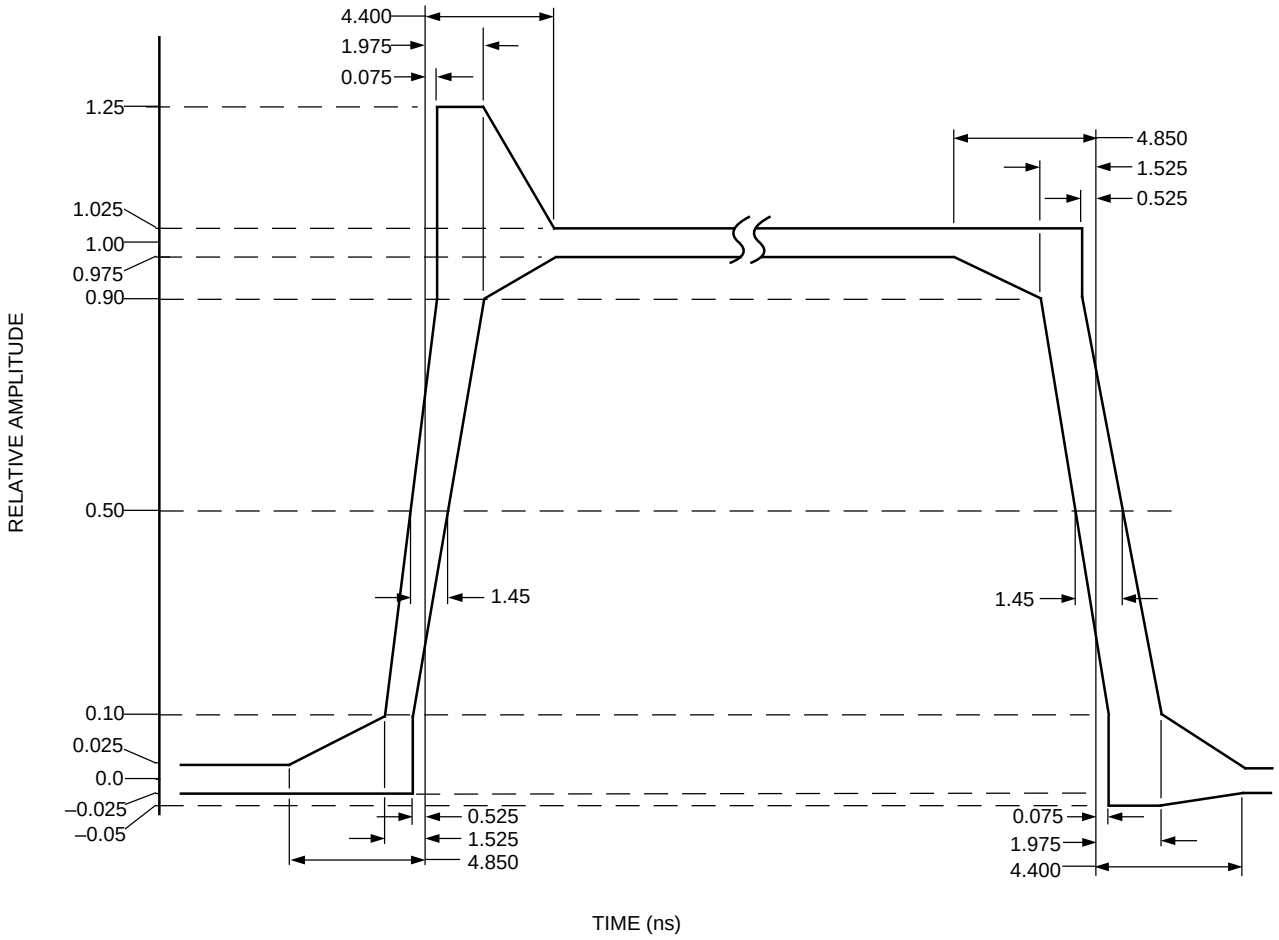


Figure 2. Pulse Envelope

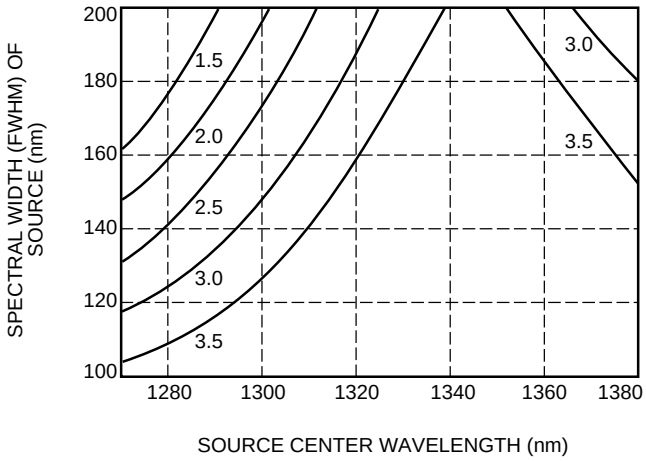


Figure 3. Spectral Width

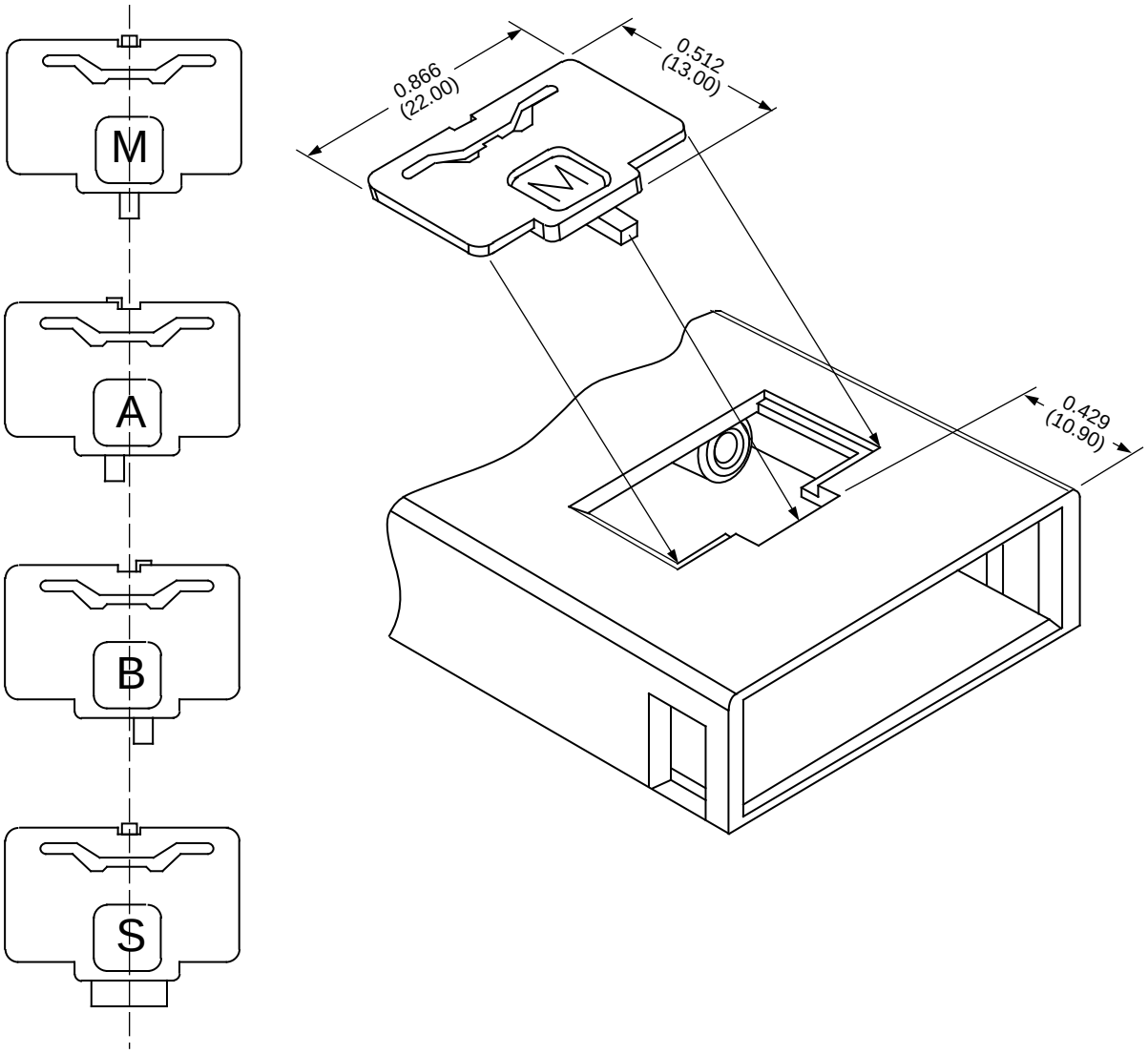
Keying Configurations

To insert the key in the receptacle:

1. Choose the appropriate key (A, B, M, or S).
2. Insert the tabbed end (labeled end) of the key through the opening in the top of the receptacle, and fit in place.
3. Push the back end of the key down until it snaps into place. The key seats flush to below flush with the top of the transceiver.

To remove the key from the receptacle:

1. Place the tip of a small, flat screwdriver in the slot at the back of the key.
2. Gently but firmly exert pressure on the key by prying back on the screwdriver.
3. Remove the key.



Note: Dimensions are in inches and (millimeters).

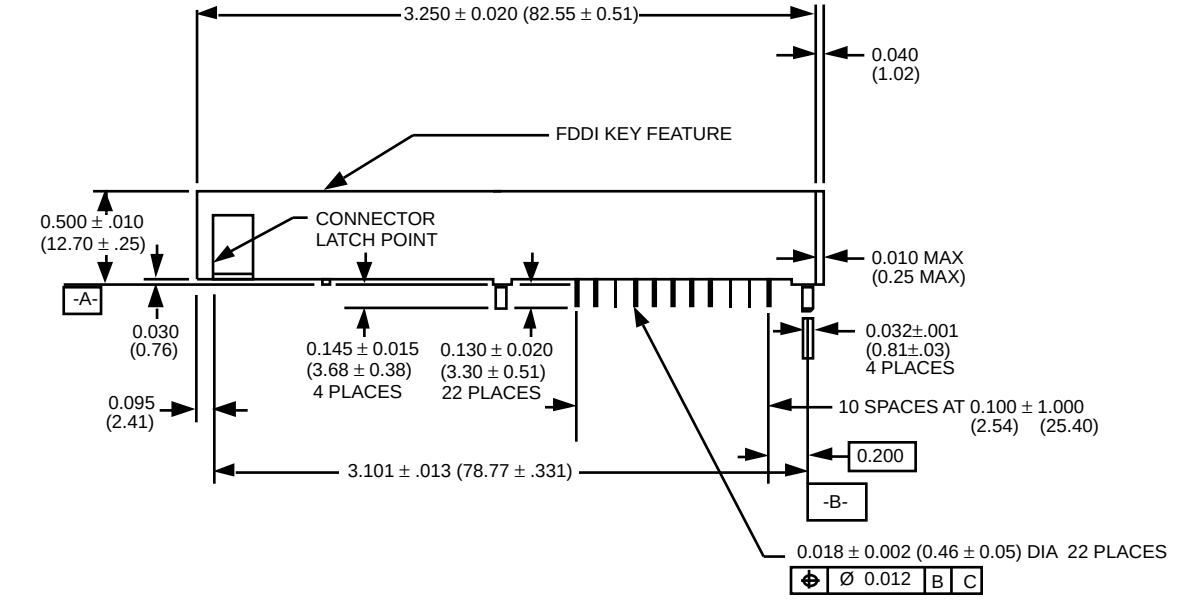
Figure 4. Keying Configurations

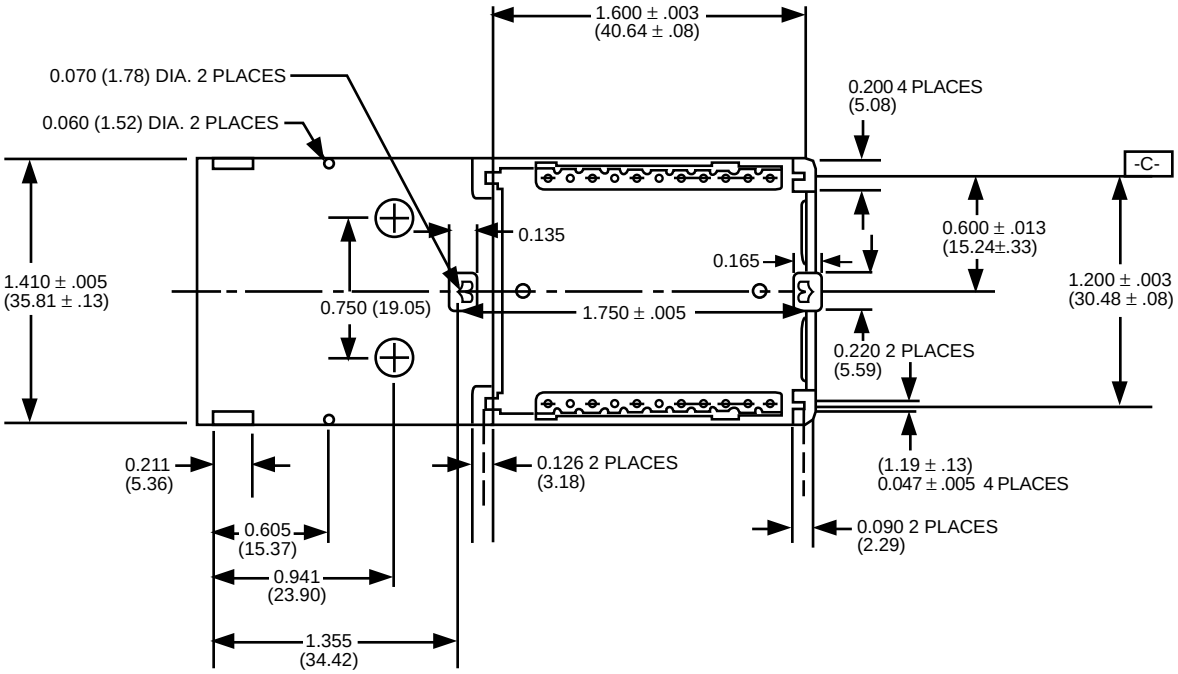
Outline Diagrams

Dimensions are in inches and (millimeters).

All dimensions are reference unless tolerances are specified.

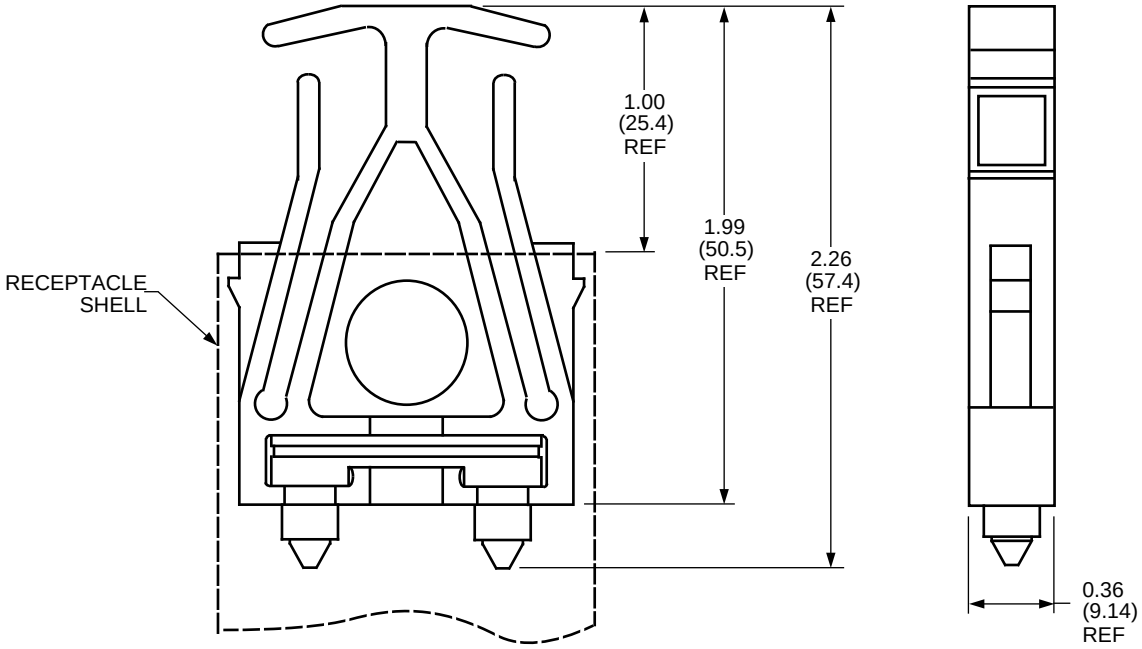
1402C Transceiver





Outline Diagrams (continued)

1402C Process Plug



Ordering Information

Table 3. Device Information

Device	Code	Key
FDDI Transceiver	1402CA	A
	1402CB	B
	1402CM	M
	1402CS	S
	1402C	*
FDDI Insert Keys:		
Bag of 100 A Keys	—	A
Bag of 100 B Keys	—	B
Bag of 100 M Keys	—	M
Bag of 100 S Keys	—	S
Bag of 100 Sets of A, B, M, S Keys	—	A, B, M, S
FDDI Process Plug (bag of 100)	—	—

* Unkeyed/universal. The transceiver is shipped with one set of FDDI insert keys. The customer has the option of keying the transceiver. See Keying Configurations section.

Order From

Or for additional information, contact your local CTS Distributor, Agent, Sales Representative or in:

U.S.A., EUROPE, ASIA PACIFIC:

CTS Microelectronics, 1201 Cumberland Avenue, W. Lafayette, Indiana 47906
Phone 317-463-2565, FAX 317-497-5399

JAPAN:

CTS Corporation, Japan Sales Office, Mori Building No. 32, 4F, 4-30, 3 Chome Shibakoen, Minato-ku Tokyo 105, Japan
Tel. 81-3-5472-6201, Fax 81-3-5472-6234

Revised April, 1996
DS92-195LWP