ODL® 125 Series II Lightwave Data Link

Features

- FDDI compliant
- Low-cost plastic package design
- 16-pin package with *ST*® Receptacle
- Small size
- High reliability
- Low power dissipation
- Single power supply
- Ambient operating temperature range: 0 °C to 70 °C
- 100K ECL compatible
- Single-detect indicator
- Data link immunity to EMI/RFI, crosstalk, and ground loops

The *ODL* 125 Series II Data Link provides electrical isolation and intrusion-resistant data transmission between systems at speeds up to 125 Mbits/s. (Transmitter is shown in nonconductive package.)

Description

The *ODL* 125 Series II Lightwave Data Link is a high-performance link that operates at data rates from 20 Mbits/s to 125 Mbits/s (NRZ) at a typical distance of 3 km. The link has a typical power margin of 20.9 dB BOL (beginning of life). A 13.0 dB power margin is predicted for worst-case conditions over 50,000 hours. Complementary bipolar integrated circuits are used to achieve high data rates.

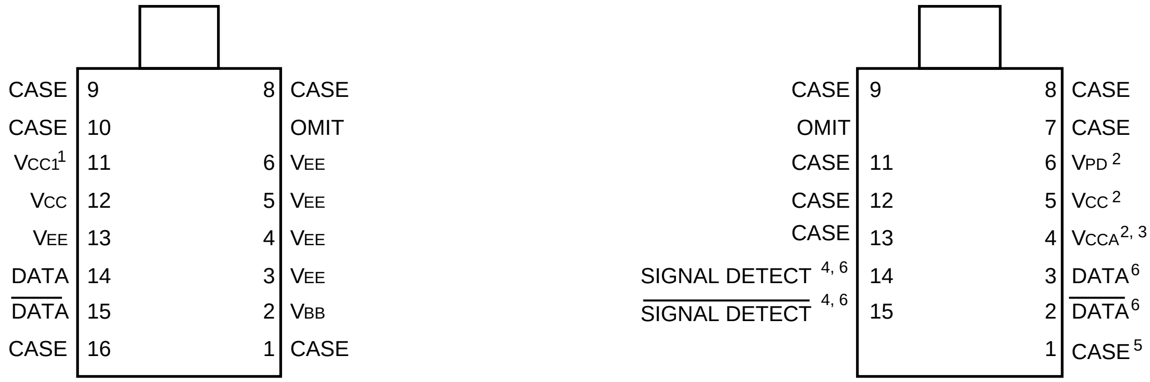
All of the devices are housed in 16-pin DIPs to mate with *ST* Connectors. The link is optimized for 62.5/125 µm fiber but can be used with 50/125 µm, 85/125 µm, and 100/140 µm fibers as well.

The transmitter consists of a long-wavelength, high-speed LED and a silicon IC. The device operates from a positive power supply (V_{CC} = 4.5 V to 5.5 V).

The receiver is equipped with a PIN photodetector and includes components similar to those in the transmitter. It also operates from a positive power supply (V_{CC} = 4.5 V to 5.5 V). The receiver housing is manufactured from a conductive plastic material which reduces the data link's susceptibility to radiated EMI and RFI fields. (Non-conductive plastic is available.)

Pin Information

Top view.



A. Transmitter Pin Diagram[7] **B. Receiver Pin Diagram**

1. V_{CC1}: LED supply voltage normally set equal to V_{CC}.
2. Voltages on V_{CC}, V_{PD}, and V_{CCA} must be set equal. V_{CC}, V_{PD}, and V_{CCA} should each be filtered separately from a common supply.
3. V_{CCA}: positive supply for output logic states.
4. SIGNAL DETECT is a logic signal that indicates the presence or absence of a minimum acceptable level of optical signal input. (A logic-high on SIGNAL DETECT indicates presence of a signal.)
5. All case pins are internally connected to logic common (ground).
6. DATA, $\overline{\text{DATA}}$, SIGNAL DETECT, and $\overline{\text{SIGNAL DETECT}}$ are open-emitter circuits.

Figure 1. Pin Diagrams

Printed-Wiring Board Layout

As with any sensitive or high-speed electronic component, to obtain optimum performance from fiber-optic data links, careful attention must be given to the printed-wiring board. The routing of sensitive input traces relative to other components and signal lines must be considered in great detail. Data lines must be of controlled impedance and properly terminated to minimize reflections which might degrade performance. Power supply pins must be protected from noisy operating conditions by proper filtering.

Printed-Wiring Board

As a minimum, a double-sided printed-wiring board having a large ground plane on the component side should be utilized. In applications where a large number of other devices are included on the circuit card, a multilayer circuit board is preferred. This allows for the separation of power and ground connections, and provides isolation for sensitive traces from high-level signals which might couple to the sensitive inputs.

In either case, the ideal approach is to have the ground plane as close to the data links as possible and to cover as much of the printed-wiring board as possible.

Printed-Wiring Board Layout (continued)

Layout Considerations

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. It is designed to detect and amplify signal levels that are only nanoamperes in amplitude. Any unwanted signals which couple into the receiver circuitry will cause a decrease in the receiver's sensitivity and may also degrade the performance of the receiver's signal detect indicators.

To minimize the coupling of unwanted noise into the receiver, transmitter input traces and other traces carrying high-level signals should be routed as far away as possible from the receiver pins. If wide separation of the receiver pins from other high-level signal lines is not possible, then the receiver pins and traces connected to them should be shielded by placing a ground trace between the receiver's pins and connecting traces and other high-level signal paths.

Power Supply Filtering

Noise that couples into the devices through the power-supply pins can also degrade device performance. Figure 2 shows the recommended power-supply filtering for the transmitter, and Figure 3 shows the same for the receiver power-supply pins. The 0.1 µF capacitors should be high-quality ceramic devices rated for RF applications. Place the capacitors as close as physically possible to the VCC pins. The ideal situation is surface-mount capacitors mounted up against the power-supply pins.

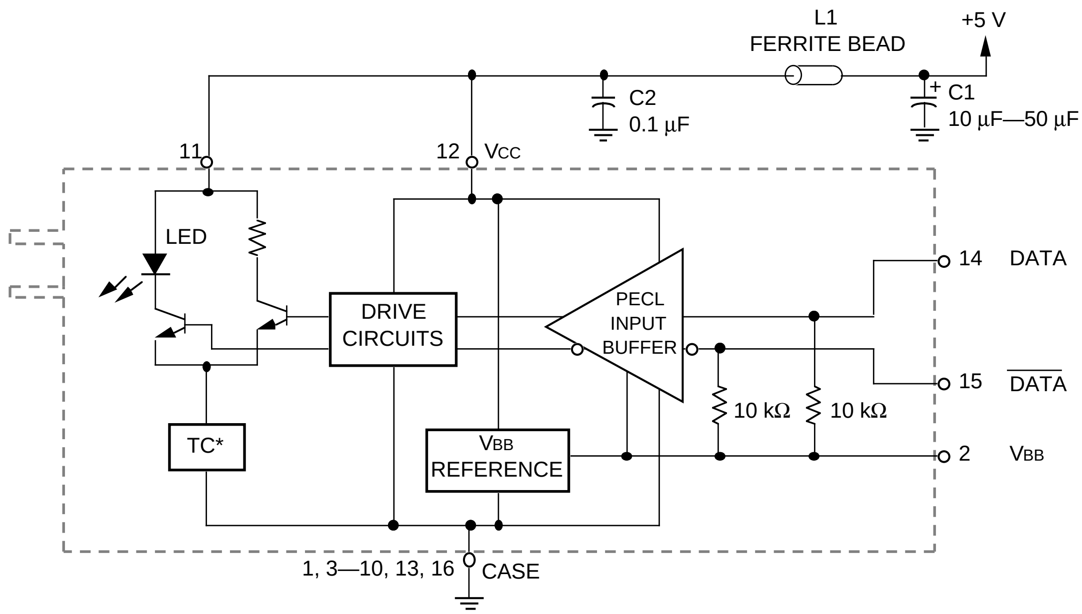
In some instances, especially on double-sided circuit boards in noisy environments, it may be necessary to provide separate filtering for the VPD bias pin on the receiver. Do this by placing a separate 0.1 µF capacitor from pin 6 to ground, and connecting pin 6 to VCC through a separate ferrite bead.

Data Lines

The signals on the data lines typically have rise and fall times on the order of 1 ns to 2 ns. If the data lines are not properly handled, the fast transitions cause EMI problems as well as electrical reflections and excessive ringing, which degrade the performance of the transceiver. When laying out the traces for the data lines, follow high-speed ECL design guidelines as described in the *Motorola MECL System Design Handbook.*

- All high-speed output lines must use controlled-impedance traces and have the termination impedance match the trace impedance. Controlled-impedance interruptions must be avoided (i.e., 90° bends, etc.), and paired lines (i.e., DATA and $\overline{\text{DATA}}$) should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination resistor.
- Data and signal-detect output lines should be as short and straight as possible and should be isolated from noise sources (and each other) to prevent noise from feeding back into the receiver.

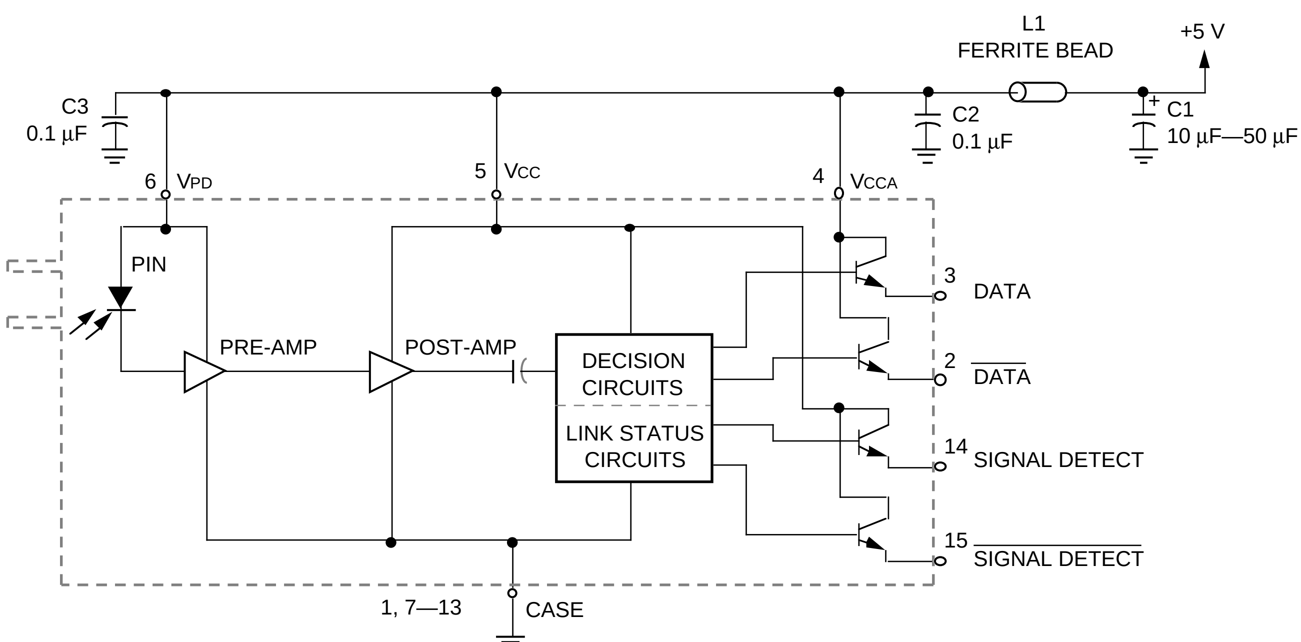
Printed-Wiring Board Layout (continued)



* Temperature compensated bias circuits.

Notes:
L1 — Ferrite bead: Fair-Rite Products Corp., part number 27430021111 or equivalent.
C1 — Tantalum electrolytic capacitor.
C2 — High-quality ceramic capacitor placed as close as possible to supply-voltage pins.

Figure 2. Transmitter Block Diagram and Recommended Power Supply Filtering



Notes:
L1 — Ferrite bead: Fair-Rite Products Corp., part number 27430021111 or equivalent.
C1 — Tantalum electrolytic or equivalent.
C2, C3 — High-quality ceramic capacitor placed as close as possible to supply-voltage pins.

Figure 3. Receiver Block Diagram and Recommended Power Supply Filtering

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–40	100	°C
Lead Soldering Temp/Time*	—	—	240/10	°C /s
Supply Voltage†	—	0	6.5	V
Output Current‡	I_O	—	50	mA
Input Voltage§	V_I	V_{EE}	V_{CC} + 0.5	V
Differential Input Voltage	—	—	2.0	V

* Applies to pins only.
† Measured from V_{EE} to V_{CC}.
‡ From DATA and $\overline{\text{DATA}}$ outputs of receiver.
§ Voltage at DATA or $\overline{\text{DATA}}$ input terminals of transmitter measured from V_{CC}.

Data Link Processing

The *ODL* 125 II Data Link devices are not hermetically sealed and should not be totally immersed in liquids. However, the devices have a sealed OSA and are potted. When used in conjunction with the connector process caps that are placed on every unit prior to shipment, they are wave-solderable and cleanable with water and detergent only. The recommended cleaning procedure is a high-pressure wash with an aqueous (soap and water) solution. The wash should be followed by several high-pressure rinses applied through a series of nozzles or manifold slots. After several rinse cycles, the devices should be completely dried. Since there are variations in wave soldering and cleaning methods, the process caps performance should be tested with each customer’s process.

Installation Considerations

The data links are designed to be, and have proven to be, rugged devices; but, as in any precision device, care should be used during handling. When mating/ demating with a connector, an obvious push-twist-pull is used, but excessive force should be avoided. The maximum mating/demating force should not exceed 3 lbs.

It is important to keep the connector ferrule and data link optical port free from dust. The process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present in the optical port, the use of canned air with an extension tube should remove any debris.

Qualification Testing

The 1261 BCE and 1361 BCE have successfully passed the following qualification testing:

Parameter	Conditions	Sample Sizes/Failures	Failure Criteria
Physical Dimensions	MIL-STD-883C-2016	93/0	Visual
External Visual	MIL-STD-883C-2009.8	93/0	Visual
Impact Shock	1500G, 5 hits, 6 axis, MIL-STD-883C-2002.3	22.0	Electrical/optical
Variable Frequency Vibration	20G, 10Hz to 2kHz, 4 cycles, 3 axis, 4 minutes/cycle, MIL-STD-883C-2007.1	22/0	Electrical/optical
Solderability	MIL-STD-883C-2003.5	5/0	Qualified by product similarity
Lead Integrity	MIL-STD-883C-2004.5	5/0	Visual
Marking Permanence	MIL-STD-883C-2015.7	5/0	Qualified by product similarity
Temperature Cycle	–40 °C to + 130 °C, 5 cycles	93/0	Electrical/optical
Temperature Cycle	–40 °C to + 130 °C, 1000 cycles MIL-STD-883C-1010.7	11/0	Electrical/optical
High Temperature, High Humidity, with Bias	85 ° C, 85% relative humidity, rated bias, 2000 hours	30/0	Electrical/optical
HighTemperature, with Bias	100 °C ambient, rated bias, 2000 hours, MIL-STD-883C-1005.5	30/0	Electrical/optical
Power Cycle	Combined with high temperature, high humidity with bias; 1000 on/off cycles over 2000 hrs.	30/0	Electrical/optical
Internal	MIL-STD-883C-2014	11/0	Visual
Electrostatic Charge	Human-body model (to determine class)	5	See ESD Classification

Handling Precautions

Electrostatic Discharge (ESD) Classification

CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the device, take proper precautions (i.e., wear grounding wrist straps) to prevent ESD damage.

CTS employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

The ESD classification of the *ODL* 125 II has been evaluated as follows:

Test Method	Classification	
	1261BCF	1361BCF
MIL-STD-883, Method 3015.5	Class 1	Class 2

Fiber Size Considerations

Although optimized for 62.5/125 µm fiber, the *ODL* 125 II can be used with alternate fiber sizes. Testing of the *ODL* 125 data links has confirmed the accuracy of Table C.3 of the ANSI X3.166 FDDI PMD specifications for determining adjustments to loss budget if used with an alternate size.

Electrical Characteristics

Table 1. Transmitter Characteristics

Transmitters are FDDI compatible over the following conditions: VCC – VEE = 4.5 V to 5.5 V; ambient operating temperature: 0 °C to 70 °C; complementary inputs.[1]

Parameter	Symbol	Min	Typ	Max	Unit
Input Data Voltage:[3]					
Low	V_{IL}	–1.810	—	–1.475	V
High	V_{IH}	–1.165	—	–0.880	V
Input Current:					
Low[4]	I_{IL}	0.4	—	—	mA
High[5]	I_{IH}	—	—	0.4	mA
Reference Voltage[6]	V_{BB}	–1.396	–1.320	–1.244	V
Input Transition Time[7,8]	t_I	0.5	—	3.0	ns
Power Supply Current	I_{CC}	—	134	150	mA
Data Rate (NRZ)	DR	20	—	125	Mbits/s
Average Optical Power[9,10]	P_O	15.8(–18.0)	25.7(–15.9)	39.8(–14.0)	μW(dBm)
Disable Power (Input Low)[11]	P_{OL}	—	0.003(–55.0)	0.03(–45.0)	μW(dBm)
Dynamic Extinction Ratio[7,12]	EXT_S	—	2.0	10.0	%
Static Extinction Ratio	ER	31.5	—	—	dB
Output Rise Time[7,13]	t_R	0.6	1.1	3.5	ns
Output Fall Time[7,13]	t_F	0.6	2.1	3.5	ns
Optical Wavelength (center)	λ_C	1270	1312	1380	nm
Spectral Width (FWHM)	Δ	—	122	200	nm
Power Dissipation[14]	P_{DISS}	—	0.67	0.83	W
Data-dependent Jitter[15]	DDJ	—	0.2	0.6	ns (p-p)
Random Jitter[16]	RJ	—	0.3	0.7	ns (p-p)
Duty-cycle Distortion[16]	DCD	—	0.2	0.6	ns (p-p)

1. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-endedly.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges, unless otherwise noted.
3. Measured at 25 °C from V_{CC} with a 50 Ω load to (V_{CC} – 2.0 V).
4. Measured with V_{IL} at minimum.
5. Measured with V_{IH} at maximum.
6. Measured from V_{CC}.
7. Measured with the FDDI specified halt-line-state input (12.5 MHz square wave).
8. Between 20% and 80% points.
9. The minimum value given is at the beginning of life, at 25 °C ambient temperature, and under normal operating conditions.
10. Measured average power coupled into 0.275 NA, 62.5/125 μm fiber.
11. The optical output power with a logic-low at the input.
12. Ratio of the optical power in the logic-low state to the optical power in the logic-high state.
13. Between 10% and 90% points.
14. Maximum value specified with a 5.5 V power supply voltage.
15. Measured output jitter with a 125 Mbits/s input, worst-case data pattern specified in FDDI PMD Appendix A, having negligible DDJ.
16. Measured with a 125 Mbits/s input 1010 pattern having negligible DCD or random jitter.

Electrical Characteristics (continued)

Table 2. Receiver Characteristics

Receivers are FDDI compatible over the following conditions: VCC = 4.5 V to 5.5 V; ambient operating temperature: 0 °C to 70 °C; complementary outputs.[1]

Parameter	Symbol	Min	Typ	Max	Unit
Output Data Voltage:[3]					
Low	V_{OL}	–1.810	–1.70	–1.620	V
High	V_{OH}	–1.025	–0.95	–0.880	V
Current Drain on VCC	I_{CC}	—	120	130	mA
Curren Drain on VCCA[4]	I_{CCA}	—	25	35	mA
Data Rate (NRZ encoding)	DR	20	—	125	Mbits/s
Eyewidth[5]	EW	2.1	5.0	8.0	ns
Average Optical Sensitivity[6]	P_I	—	0.21(–36.8)	0.50(–33.0)	µW(dBm)
Average Maximum Input Power[7]	P_{MAX}	39.8(–14.0)	74.1(–11.3)	—	µW(dBm)
Optical Wavelength for Rated Sensitivity	λ	1270	—	1380	nm
Output Rise Time[8, 9]	t_R	0.5	1.4	2.5	ns
Output Fall Time [8,9]	t_F	0.5	1.4	2.5	ns
Power Dissipation[10]	P_{DISS}	—	0.65	0.72	W
Output Signal-detect Voltage:[3,11]					
Low	V_{FL}	–1.810	–1.70	–1.620	V
High	V_{FH}	–1.025	–0.95	–0.880	V
Signal-detect Assert Level[11] (average power, increasing light input)	S_{DAL}	–41.5	–36.0	–31.5	dBm
Signal-detect Deassert Level[11] (average power, decreasing light input)	S_{DDL}	–43.0	–38.5	–34.0	dBm
Signal Detect: Hysteresis[11]	HYS	1.5	2.5	3.5	dB
Signal-detect Timing:					
Assert[12]	S_{DTA}	—	25	100	µs
Deassert[13]	S_{DTD}	—	33	350	µs
Data-output Timing:					
Assert[14]	D_{TA}	—	<1	15	µs
Deassert[15]	D_{TD}	12	25	—	µs
Duty-cycle Distortion[16]	DCD	—	0.1	0.4	ns (p-p)

1. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved by using either output individually.
2. Minimum and maximum values are guaranteed over specified voltage and temperature ranges, using bypass network (Figure 3).
3. Measured at 25 °C from V_{CC} with a 50 Ω load to (V_{CCA} – 2.0 V).
4. With 50 Ω loads on DATA, $\overline{\text{DATA}}$, SIGNAL DETECT, $\overline{\text{SIGNAL DETECT}}$ tied to (V_{CC} – 2.0 V).
5. During an 8 ns bit-period, eyewidth is the time span in which the bit error rate is less than 2.5×10^{-10}. Eyewidth is measured with a 125 Mbits/s optical input by using the data pattern specified in Appendix A of the FDDI PMD. An average optical power of –31.0 dBm is used for the receiver. The input is coupled from a 0.275 NA, 62.5/125 µm fiber.
6. Average optical power coupled from a 0.275 NA, 62.5/125 µm fiber at 125 Mbits/s with a $2^7 - 1$ pseudorandom data pattern at a 50% duty cycle for a bit error rate of 2.5×10^{-10} (optimum sensitivity with 0 eyewidth).
7. The maximum average input power corresponds to a minimum eyewidth of 2.1 ns at 2.5×10^{-10} bit error rate (BER).
8. Specified at a 125 Mbits/s data rate.
9. Between the 20% and 80% points with a 50 Ω load to (V_{CC} – 2.0 V).

Electrical Characteristics (continued)

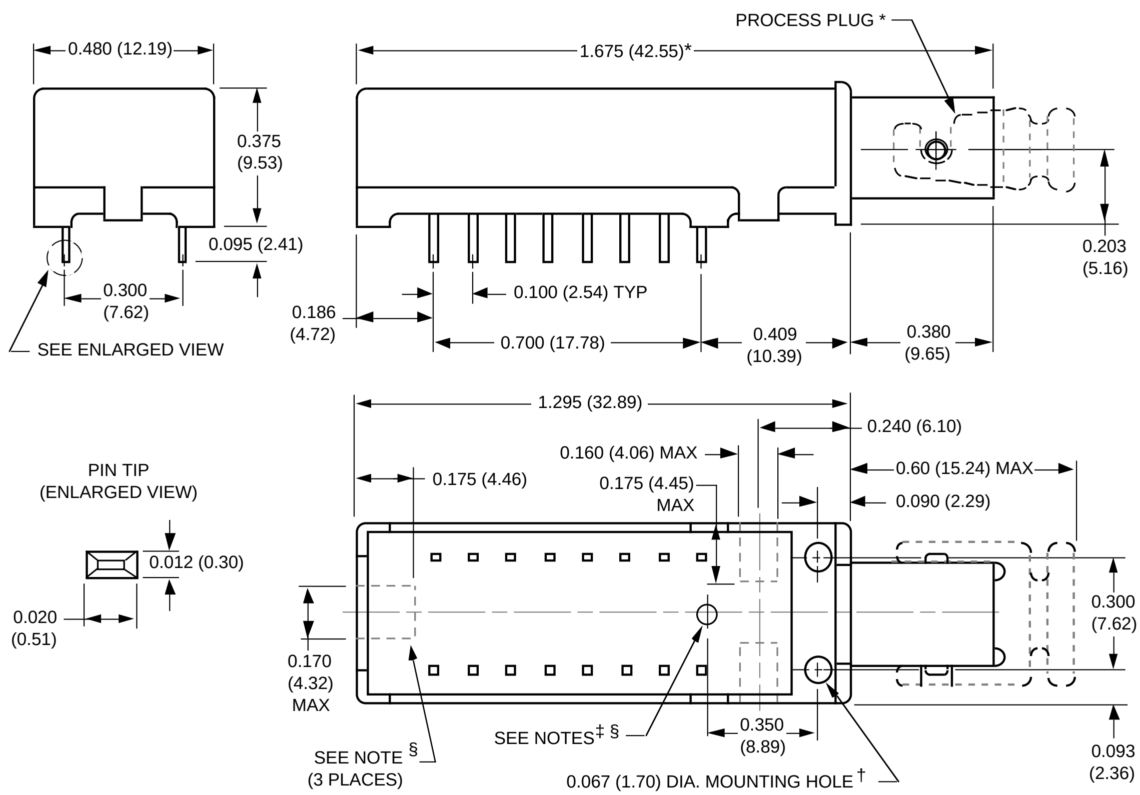
Table 2. Receiver Characteristics (continued)

10. With a +5.5 V power supply, 50% duty cycle, and logic outputs terminated in 50 Ω to (V_{CC} – 2.0 V).
11. SIGNAL DETECT is logic 1 for light input levels above the indicated switching level and logic 0 for input levels below the indicated switching level. Whenever the signal detect is asserted, the BER of the data outputs is less than or equal to 0.01.
12. The value specified is the maximum time it takes the signal detect to assert after a step increase in the optical power into the receiver (measured with the data pattern specified in Appendix A of the FDDI PMD).
13. The value specified is the maximum time it takes the signal detect to deassert after a step decrease in the optical power into the receiver (measured with the data pattern specified in Appendix A of the FDDI PMD).
14. The value specified is the maximum time before the receiver data outputs reflect a BER of better than 0.01 (measured starting after the signal detect's assertion).
15. The value specified is the minimum time before the receiver data outputs reflect a no-light condition with a BER of 0.01 or worse (measured from the time the receiver begins receiving a no-light input).
16. Measured with a 125 Mbits/s input 1010 data pattern having negligible duty-cycle distortion.

Outline Diagrams

Dimensions are in inches and (millimeters).
Transmitter weight: 5.5 g. Receiver weight: 5.5 g.

CAUTION: These components are not hermetically sealed. Do not totally immerse in solvents.



* Process plug will extend overall length by 0.30 (7.62) beyond connector end.
† Use a #1 self-tapping screw. Insert screw before soldering module on PWB. Maximum length = 0.3 in. + circuit board thickness.
‡ Data link receivers have a soldered, internal ground connection at this location. Do not place nonground vias or traces within 0.075 inches (1.91 mm) of this location. Transmitters do not have this feature.
§ Do not place signal or power supply metal within areas around solder tabs or internal ground connection. Metal shield and plastic housing are at ground potential.

Notes:
Pin 7 is missing on the 1261 BCE Transmitter, and pins 10 and 16 are missing on the 1361 BCE Receiver.

The dimensions shown are all nominal values. For detailed dimensions, contact a CTS Applications Engineer.

Ordering Information

Table 3. Ordering Information

Device	Part Number
ODL 125 Series II Transmitter	1261 BCE
ODL 125 Series II Receiver	1361 BCE
ODL 125 Series II Transmitter (Non-Conductive)	1261 BCE1
ODL 125 Series II Receiver (Non-Conductive)	1361 BCE1

Notes

Order From

Or for additional information, contact your local CTS Distributor, Agent, Sales Representative or in:
U.S.A., EUROPE, ASIA PACIFIC:
CTS Microelectronics, 1201 Cumberland Avenue, W. Lafayette, Indiana 47906
Phone 317-463-2565, FAX 317-497-5399
JAPAN:
CTS Corporation, Japan Sales Office, Mori Building No. 32, 4F, 4-30, 3 Chome Shibakoen, Minato-ku Tokyo 105, Japan
Tel. 81-3-5472-6201, Fax 81-3-5472-6234

August 1992, Revised January 1996
DS92-081LWP (Replaces DS90-166LWP) 7.5M-12-94B