New generation CCD controller requirements and an example: the San Diego State University generation II controller

Robert Leach, Frank Beale and James Eriksen

Dept. of Astronomy, MS 1221, San Diego State University
San Diego CA 92182 e-mail: leach@mintaka.sdsu.edu,
fbeale@mintaka.sdsu.edu, jamey@mintaka.sdsu.edu

ABSTRACT

New generation astronomical CCD controllers are being required to operate a variety of CCDs in a range of ground-based applications. These include simultaneous readout from two or four corners of the same CCD (multiple readout), operation of several CCDs in the same focal plane (mosaics), fast readout of small devices for wavefront sensing in adaptive optics systems, readout of only a small region or number of regions of a single CCD (sub-image or region of interest readout), merging the charge from neighboring pixels before readout (binning), continuous readout of devices for drift scan observations, and low contrast polarimetric or spectroscopic differential imaging. Most astronomical applications require that the controller electronics not contribute significantly to the readout noise of the CCD, that the dynamic range of the CCD be fully sampled , that the CCD be read out as quickly as possible from one or more readout channels, and that some flexibility in readout modes and device format exist. A further requirement imposed by some institutions is that a single controller design be used for all their CCD instruments to minimize maintenance and development efforts. The Generation II controller design recently completed at San Diego State University to address these requirements is reviewed. A user-programmable digital signal processor (DSP) operating as a sequencer and communications processor is combined with 12-bit digital-to-analog converters for setting all CCD voltages, a video processor chain with speeds of up to 1 MHz, 16-bit analog-to-digital converters, and a bussed backplane architecture for incorporating the control and readout of multiple CCDs by replicating the clock driver and video processing elements.
Keywords: CCDs, optical astronomy

1. INTRODUCTION

Most early astronomical CCD cameras were used for direct imaging applications, and broad-band filters were often used with fairly long exposure times so the high sky and object photon fluxes resulted in enough detected photons that their Poisson counting noise dominated the high readout noise of early CCD devices[1,2]. Early CCDs had only a single readout circuit because their small area made the image readout time acceptable for most applications, and most instruments contained only a single CCD because of the difficulty and expense of acquiring good quality CCDs. In these cameras a simple readout protocol was utilized: at the end of the exposure the charge from each CCD pixel was transferred in sequence to the readout circuitry, whose output numbers were displayed and analyzed in the same geometry as the CCD image plane. The flexibility of these cameras was generally limited to having jumpers that could be set to the number of rows and columns to be read out so they could be used with different format sensors. These cameras contained a controller that consisted of the circuits to drive the CCD clocks, a video processor, an analog-to-digital (A/D) converter and a digital waveform generator (or sequencer), and were typically implemented with simple digital logic circuits, often on hand-wired boards that were expensive to duplicate.

With the success of these early cameras in ground-based astronomical observations and the improved performance of available CCDs in the late ’70s and early ’80s came a proliferation of instruments with CCDs detectors and a parallel invention of several innovative operating modes to address a diversity of observational requirements. These included spectrographs[3], drift scanning direct imagers [4,5], differential imagers for polarimetry [6], the operation of multiple CCDs in a single focal plane (mosaics)[7], and star trackers[8]. To operate CCDs in these modes several controllers were designed that were programmable to varying degrees, the most versatile ones typified by Marcus, et. al.[9] and Jorden, et al.[10]. More recent innovations have been the implementation of several

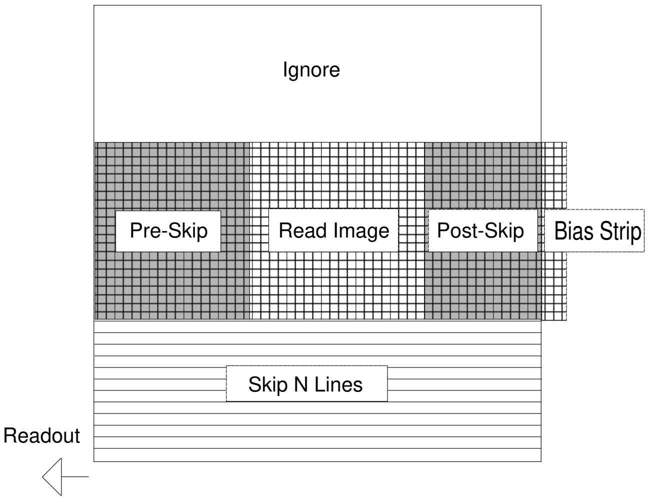

Fig. 1 - Sub-image readout with bias stripe. The readout direction is to the bottom and left to the lower left hand

readout circuits on a single CCD[11] and the use of CCDs as wavefront sensors in adaptive optics systems[12]. In section 2. below each of these operational modes will be described in more detail to illustrate the way in which the CCDs can be controlled.

Parallel to this evolution of CCD operational modes has been an evolution in the performance of CCD sensors in the astronomical important areas of readout noise, readout speed and number of pixels per device. Other areas of CCD performance of importance to astronomical applications such as dark current, quantum efficiency and charge transfer efficiency that have little bearing on controller performance will not be discussed. The readout noise of CCDs has declined markedly over the years, and recent announcements indicate low readout noise at fast readout speeds has been achieved. There has also been a dramatic increase in the number of pixels per CCD from of order 10^4 twenty years ago to of order 10^7 now. These three parameters place new demands on controllers operating recently developed astronomical CCDs, especially if they are to operate in a diversity of operational modes.

2. ASTRONOMICAL READOUT MODES

Perhaps the simplest variation on simple whole image readout is drift scan[4,5]. The scene to be observed is allowed to drift across the image plane of the CCD while each line of the CCD is clocked at the same rate at which the image is drifting. Typically the telescope tracking is just turned off and the image is read out at the sidereal rate. Every pixel in a given column detects light from the same piece of the sky and contributes to the final image. Variations in the pixel-to-pixel sensitivity are smoothed out, rendering flat-field corrections simpler and more accurate. The controller required for this readout is just a bit more sophisticated - the command to read a line needs to be synchronized to an external clock.

More sophisticated than drift scan is sub-image readout, wherein only a portion of the CCD is read out, the rest being simply discarded. Fig. 1 shows a cartoon of this process. The portion of the image to be read is shown at the center, and a bias strip for calibration is also shown as needing to be read out. The N lines below the area to be read out can be skipped over very quickly by executing a cycle of parallel clocks for each line. This time is typically a few tens of microseconds compared to a time to read each line of several tens of milliseconds, so a significant readout time decrease results. At the end of skipping the N lines the charge built up in the serial register needs to be cleared out by executing a cycle of serial clocks, one cycle for each column in the CCD. The cycle time for serial clocks is a few hundred nanoseconds for typical astronomical controllers and CCDs, which is much shorter than a typical pixel processing time because the latter includes time for the signal integration and A/D conversion, which is typically several tens of microseconds. Once the readout arrives at a line containing the pixels to be read out, the parallel clocks transfer one line at a time and the number of columns in the pre-skip region shown in the figure are skipped with the fast cycling of serial clocks. The image pixels are then read normally, after which the post-skip pixels are dismissed and the bias pixels are read normally. The top of the image can be ignored as long as there is a fast clearing of the entire CCD before the next exposure begins to remove charge from the entire array. The clearing can be a series of parallel clock cycles.

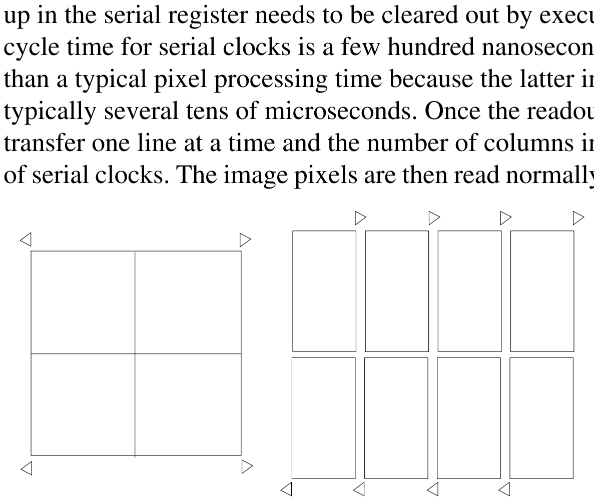

Fig. 3 - Simple schematic of a single CCD with four readouts and a mosaic consisting of eight single readout 2k x 4k CCDs.

Variations on the sub-image readout mode have been described for use in star trackers[8], wavefront sensors for adaptive optics work[12] and fast photometers[11,13]. In the wavefront sensing application shown in Fig. 2 the image is of a single star, natural or from backscatterred laser light, split into a square array of stellar images, shown as 7 x 7 in the figure. The optics are adjusted so each stellar image lies close to the center of small four pixel squares so they can be used in a quadrant

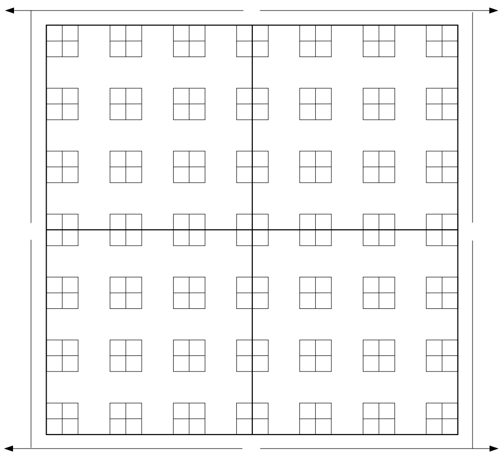

Fig. 2 - Schematic of an array of 7 x 7 stellar images from a wavefront sensor focal plane.

algorithmn to measure their centroid position. This needs to be done several hundred times a second at low readout noise in typical applications. The CCD controller is programmed to skip the regions in between the square boxes in the figure, which can be done at high speed, and only read out the four pixels in each square. Lines without stellar images are discarded with the fast parallel clocking, whereas columns not containing stellar images must be skipped over one at a time.

Multiple readout CCDs have been manufactured for many years. They are described in a recent context[11], and a review of current mosaic projects was presented by Luppino[14]. The geometry of systems described in these two references is shown in Fig. 3, to dramatize the challenge to controllers. The top of the figure shows the arrangement for four readouts on a single CCD, each at a corner. The geometry is a bit simpler for an eight CCD mosaic because there is only one readout per CCD shown. The challenge to controllers is simply to replicate the clock driver and video processor circuits required and to build a fast enough data system to read them out in a timely fashion.

3. KEY PARAMETERS AFFECTING CONTROLLER DESIGN

The CCDs currently being developed and implemented on ground-based telescopes differ from earlier devices in three important respects that have a bearing on controller design - readout noise, readout time and number of pixels. Pool of the EEV Ltd. company reported[15] low readout noise attained with a two stage on-chip preamplifier design. He reported 2 electrons rms readout noise at a readout time of 10 µsec per pixel and 3.5 electrons rms at 2 µsec per pixel for unthinned devices, comparable to values of 4.0 electrons rms at 2.5 µsec per pixel for thinned devices obtained by the authors. These also compare to values around 6 electrons rms for readout times of 20 µsec per pixel for some older but still widely used Loral devices and 2-3 electrons rms for some SITe devices operated at extremely long readout times of more than 200 µsec. These newer devices have a high node sensitivity in the range of 10-20 microvolt per electron, an order of magnitude higher than typical Loral and SITe devices. Also becoming available are ever larger numbers of pixels[15] as 2k x 4k devices are being incorporated in large mosaic cameras, and larger CCDs are under development.

The development of fast, low noise amplifiers is important for the practical utilization of CCDs in ground-based astronomy because it sharply reduces the readout time for the large CCDs. A single readout 2k x 4k CCD operated at the conventional readout time of 20 µsec per pixel required to get acceptable readout noise takes about 3 minutes. Operation with the newer low noise devices would reduce this by a factor of 5 to 20 seconds, allowing less time to be spent with the shutter closed reading out and more time acquiring photons through the telescope. The challenge for controllers is then to operate these newer CCDs at the speeds that they are capable in multiple readout, programmable controllers that can implement the variety of readout modes that astronomers have devised for their instruments.

4. SDSU II: CONTROLLER OVERVIEW

We developed a CCD controller targeted to astronomical ground-based applications several years ago that has been distributed to observatories worldwide[17]. A new controller design has been completed that reflects improvements in CCDs made in the last several years, with improvements targeted to faster readout speeds at lower readout noise and more efficient operation of multiple readouts.

Fig. 4 shows a block diagram of the controller design. Five different types of circuit boards reside in a controller housing. The clock driver board supplies clocking signals to the CCD, from digital timing waveforms generated by the timing board, while the video processor supplies DC biases, and filters and digitizes the video signal. A utility board supplies miscellaneous support functions for the system, and the timing board also serves as a communications hub. The controller housing generally resides relatively close to the CCD to minimize noise pickup on the cabling, though good results have been obtained with cable lengths of one meter

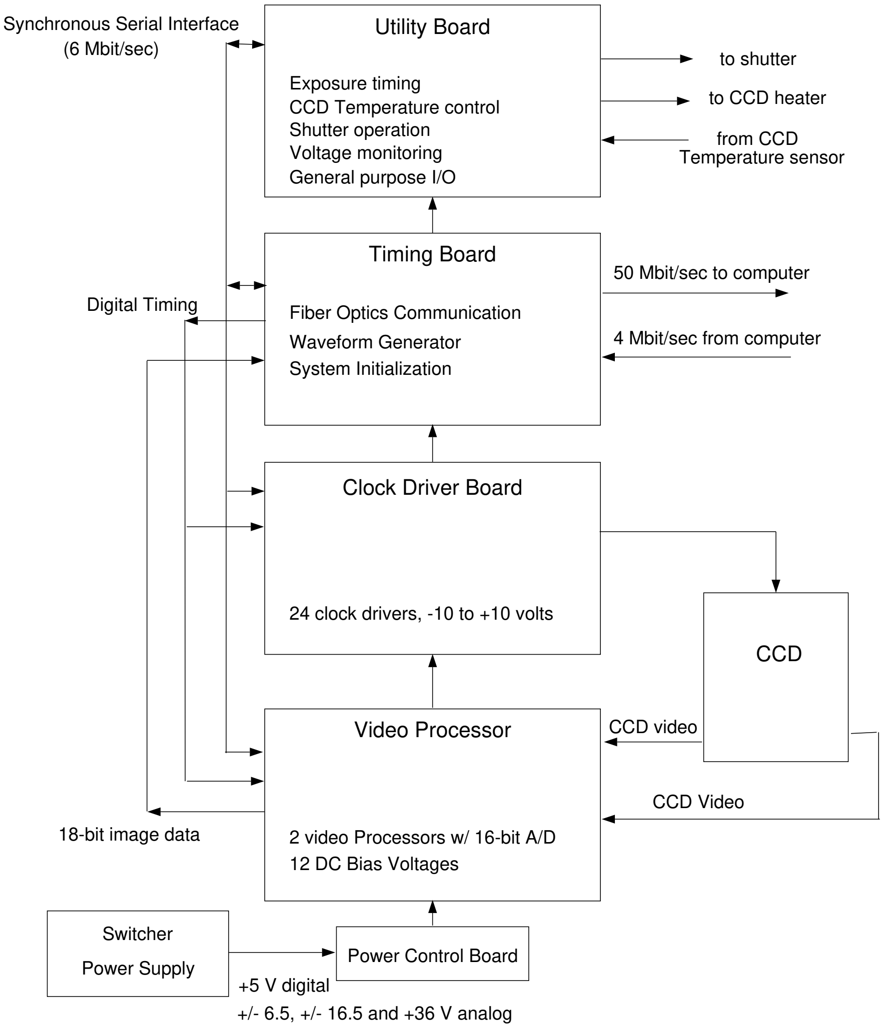

Fig. 4 - Block diagram of the main boards in a dual readout CCD controller

between the controller housing and the CCD. A power supply consisting of commercially available switcher supplies resides in a separate box that can be located several tens of meters from the controller housing. A small power control board turns on the analog voltages to the controller boards in a programmable, gentle fashion to minimize transients that might endanger the CCD or the electronics, and turns off the analog power if certain voltage and thermal conditions are not met. More than one clock driver and/or video processor board may be installed in a system, allowing the control of multiple CCDs and the simultaneous readout from more than two channels.

Communication between the host computer and the controller is over a fiber optic link to the timing board, operating at 50 Mbits/sec for transmitting data from the controller to the host computer, and 4 Mbits/sec for receiving commands from the computer. A 35-bit per word protocol is implemented for command and reply data, consisting of 24 data bits, an 8-bit header, a start bit and two stop bits. Image data are transmitted with a 19-bit protocol, consisting of 16 image bits, one start bit, and two stop bits. Image data are transmitted at a sustained rate of 2.5 Mpixels per second, a number that determines the readout rate limit for three or more readout channels. For one or two readout channels the readout rate is limited by the analog-to-digital (A/D) conversion time of 1 microsecond. The host computer can be configured either with an SBus interface board that has device driver software support for the Solaris operating on Sun Microsystems workstations, or with a VMEbus interface for more generally configured computer systems.

Power distribution and communication between the boards takes place over a commercially available VME backplane whose signal pins and timing has been redefined for this system. The boards all communicate with the DSP on the timing board via a serial link running at 6 Mbits/sec. Communication is bidirectional between the timing and utility boards, and unidirectional from the timing to the clock driver and video processor boards, being used solely for configuring the digital-to-analog converters (DACs) and slowly changing switches and multiplexers. Digital timing is provided to the clock driver and video processing boards with a time resolution of 40 nanosec over 16 signal lines over the VME backplane, with 4 bits serving as address lines to select which board is being addressed, and 12 lines being updated in each time slot. Finally, 16 image data bits are transferred in parallel from the video processor to the timing board over the VME backplane, with expandability to 18 bits in the future.

5. CONTROLLER DETAILS

A Motorola DSP56002 monolithic digital signal processor is used as the basic timing generator of the controller. The DSP functions as a timing generator by writing 24-bit data words to its data bus every instruction cycle, which are decoded by external circuitry to control various functions. Memory internal to the DSP allows a timing resolution of 40 nanosec, while memory external to the DSP has been implemented with a bank of 32k x 24-bit, no wait state SRAMs, but allows only an 80 nanosec resolution due to DSP bus traffic limitations.

To facilitate transmission of image data from multiple readouts a PAL is used to read image data from the analog-to-digital converter (A/D) converters on the video processor cards over the backplane, as it asserts six address lines to read up to 32 A/Ds. Each A/D value is read by the serial transmitter and sent over the fiber optic link, at the end of which the PAL reads the next A/D value until all of them are read. This sequence of A/D reads and transmissions is initiated with a single DSP command. This feature is implemented to allow CCD timing operations to overlap with the image data transmission.

The DSP56002 implements an emulator function called the On Chip Emulator (OnCE) via four pins on the DSP. These are brought out to a fourteen pin connector with a pinout that matches a companion board that Motorola markets for operating from a Sun, Mac or PC. The emulator can be used for a variety of debugging tasks since it allows the DSP to execute code in real time, which can be interrupted by installing breakpoints so the user can examine the contents of all internal registers and memory contents.

During CCD readout the DSP writes 24-bit timing words to the backplane. The most significant eight bits make up a delay word that postpones the execution of the next word in the waveform table by a programmable number of 20 nanosec clock cycles. The most significant bit D23 selects either a coarse or fine delay mode, wherein coarse delay sets the number D16-D22 of 160 nanosec delay steps, for delays over the range of 0.2 to 20 microsec. The fine delay selects the number D16-D23 of 20 nanosec delays, for delays over the range of 80 to 2500 nanosec. The remaining 16 bits are written to the backplane as digital timing signals for decoding by the clock driver and video processor boards.

The video processor is shown schematically in Fig. 5. It contains a low noise front end preamplifier that is AC or DC coupled to the CCD and contains a DAC controlled input offset adjustment. The preamplifier contains and Analog Devices AD829 voltage feedback, low noise op amp, chosen for its low voltage and current noise. It is a bipolar transistor op amp whose current noise and bias currents are considerably higher than similar FET op amps, but whose voltage noise is much less. Recently developed low noise, high speed CCDs have output impedances of several hundred ohms, making the current noise contribution of the AD829 op amp smaller than its already low voltage noise, especially when operated in a high gain circuit (x4) such as this one. Variations in bias current are relatively unimportant due to the short time between the sampling of the reset and signal levels in a correlated double sample circuit such as this one.

The preamplifier connects to a post amplifier through a DC restore circuit operating every pixel that has a choice of four software controlled gains over a range of x1 to x9.5. It is a low impedance driver feeding a pair of amplifiers to select the polarity of the signal input to the integrator. The output is summed on a classical integrator, followed by an A/D driver, offset adjustment and x2 gain stage . The A/D converter has 16 bits accuracy and a one microsec combined sample-hold and conversion time. A/D convert

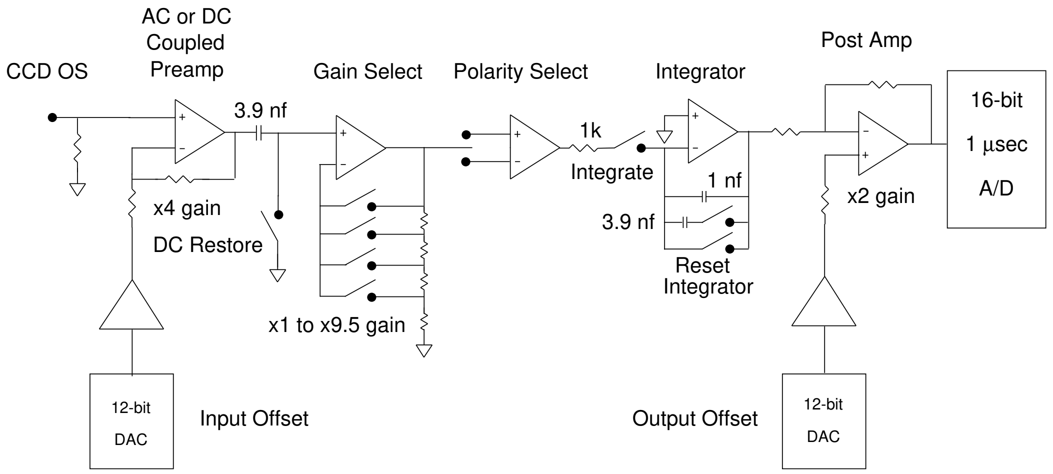

Fig. 5 - Block diagram of the CCD video processor

overlaps with all operations of the video processor board, allowing pixel processing times of one microseconds. Two identical video processors are installed on each video processor board for connection to two separate CCD readouts, with a shared PAL on the board for address decoding when reading the A/D digital output values and setting the voltages of the DACs.

Four DAC packages are provided on each video processor board, for a total of sixteen DAC circuits. Four of these are used for the offset circuits (input and output offsets on each of two video processing circuits) and the remaining twelve are split four to a CCD for generating low impedance, low noise DC bias supply voltages. Similar to the clock driver board MOSFET switches are placed between the DC bias supply drivers and the board output to disconnect the supplies from the CCD until they are fully configured during power up, or to disconnect them suddenly if there's a power failure. Either the power control board, the utility board or the timing board can turn the switches off.

The clock driver board generates 24 clocked signals over the range of -10 to +10 volts for driving CCD registers directly. Several clock driver boards may be installed in a single controller system for driving mosaics of CCDs or CCDs with complex architectures, or both. The clocks are generated by analog switches selecting from one of two voltages determined by DACs, whereby up to twelve switch states on a clock driver can be changed in a single 40 nanosec instruction cycle. The DAC voltages are updated over the serial link from the timing board, taking about 2 µsec per voltage. The clock drivers operate with a fast op amp that produces 60 mA of sustained output current, and slews over a ten volt range in 20 nanosec.

These utility board provides controller functions not directly involved in the readout, such as exposure timing, shutter control, CCD temperature control, power monitoring, and power turn on. It also has many non-dedicated analog and digital inputs and outputs that the user can customize. It operates from an interrupt service routine that executes every 800 nanosec, and uses an older style DSP56001 with extensive electrically eraseable programmable read only memory (EEPROM) program memory on board. The power control board contains five switches to turn on the analog power supplies +7, -7, +16.5,-16.5 and +35 volts from the incoming power supply cable onto the backplane where it is distributed to the video processor and clock driver boards. It turns on the power with a linear ramp lasting about ten milliseconds on command from the utility board in order to avoid power glitches from passing to the CCD that might occur with an sudden or uncontrolled power surge. It also has voltage comparators monitoring the power supply voltages to turn off the supplies if the voltages fall outside allowable limits. The digital logic on the board is powered any one of the +5, +7 and +35 volt supplies so that if all but one of them fail the board can still shut the power down gracefully. The power control board is four VME slots in width and clamps on to the back of the VME backplane. It has a large, heavy duty circular connector to the power supply.

The power supply contains commercially available switcher modules. They are encased in a fully shielded aluminum box, and contain large inductance toroids to reduce the noise generated by the switchers. Slightly lower readout noise with a fast readout, low noise CCD has been achieved with the switcher power supply than with the older linear design with a toroidal transformer. The switchers contain remote sense circuits that maintain a constant voltage at the power control board, and necessitate that remote sense wires for each of the supplies be run through the power supply cable. This enables the power supplies to be operated with a range of power supply cable lengths up to several tens of meters without adjusting the power supply voltage for ohmic losses in the cable, while the switcher power supplies are capable of operating over a wide range of input voltages and frequencies. A +5 volt supply provides power for the digital logic on the controller; +/- 7 volt power is supplied to be down-regulated to +/- 5 volts for the analog power on the A/D converters and some of the video processor op amps, while the +/- 16.5 volt power is similarly down regulated to +/- 15 volts for the A/D converters and the clock driver and video processor op amps. The +35 volt supply drives several op amps that generate up to +30 volts for the drain supplies of CCDs, and for the preamplifier op amp if configured in DC coupled mode. Two sizes of power supplies are available - a smaller one that contains four separate supplies and derives the +/- 7 volts power by down regulating from the +/- 16.5 supplies, and does not contain the remote voltage sense capability. The larger one has separate supplies for +/- 7 volts and a 12 volts fan power supply, along with remote voltage sense on all supplies except for the fan supply. The larger power supply is targeted to controllers with many video processor boards or systems that require a large distance between the controller and power supply.

6. SOFTWARE SUPPORT

DSP code that executes in the timing, utility and VME interface boards is derived from software development tools available from Motorola. An assembler, a linker, a software simulator and several format translation programs that are available on an inexpensive

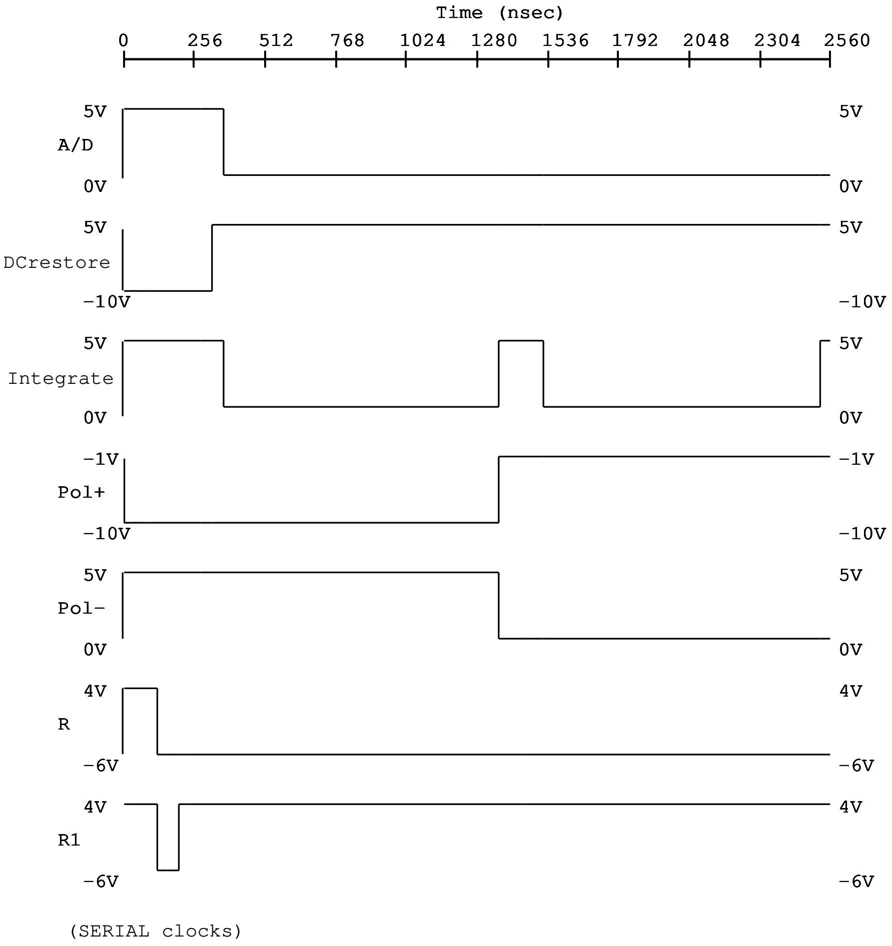

Fig. 6 - PIxel and video processing clocking waveforms generated by waveform visualization software

CDROM. DSP code for a particular board consists of two parts. Boot code to initialize the DSP, process commands, read and write from memory and communicate over the serial links is loaded into the DSP from on-board EEPROM memory after the DSP is reset. Any changes in boot code must be done by writing to the EEPROM. Application code consists of the remaining code required to operate a board, and contains such things as CCD voltage tables, timing waveforms, temperature control algorithms, and exposure timers. Application code is written to the DSP and possibly to on-board SRAM memory either by reading from the on-board EEPROM memory or by write memory commands over a communications link after booting. A typical development cycle consists of editing the application source code file with a text editor, execution of a script to assemble, link and generated a downloadable file, downloading the file from the host computer, and testing it. This cycle can take as little as a few seconds. Once the application code reaches a certain level of stability the user can write it to EEPROM memory and have the DSP read it directly.

To help the user develop timing code for reading out CCDs a waveform visualization program named Waveform has been written that reads the tables of waveform numbers from the timing board source code and plots them as a conventional timing diagram that the user can easily understand. Editing of the waveforms is still done manually by editing the numbers in the source code. Fig. 6 shows the output from the Waveform program for the video processor and some of the serial clock timing for the EEV39 CCD in a wavefront sensing application. The pixel timing is 2.56 microsec/pixel, and devotes a full 2.0 microsec of this time to integrating the video signal. It is important for achieving good noise performance at fast speeds to maximize the amount of time the video processor spends doing this integration since it directly reduces the bandwidth of the signal chain and reduces the noise. To maximize this time many operations were overlapped at the beginning of the pixel processing - all the serial clocking except for the dumping of charge onto the output node, DC restore, CCD reset, integrator reset and start A/D convert. Fast op amps with a minimum of filtering are used to minimize feedthrough of transients into the time when the signal is being integrated.

A UNIX user interface, image acquisition and display program named "ccdtool" has been written and distributed in source code form to users. It is a Solaris based, windowing program that communicates to the SBus interface board through a device driver to provide point and click specification of controller functions and control of exposures. Control over loading the application code into each DSP is provided, along with turning power on, specifying image dimensionalities, displaying images through standard display programs, recording images on disk in FITS format with a keyword editor, and running sequences of exposures.

7. PERFORMANCE SUMMARY

The table below summarizes the performance details of the controller discussed above.

Typical readout time	2.5 µsec/pixel
Fastest readout time	1.0 µsec/pixel, limited by A/D converter speed 3.2 µsec for N = 8 readouts, limited by fiber optic speed
Fiber optics	50 Mbits/sec, 400 nanosec per pixel including overhead, 2.5 Megapixels/sec sustained rate
Readout noise	<4.0 electrons rms at 2.5 µsec/pixel with EEV39 CCD
Board size	All boards are 10 x 23 cm
Boards needed for 8 readouts	9
Practical maximum of readouts	16
Computer interfaces supported	VME, SBus
A/D converter	16-bits, 1.0 µsec/pixel
Selectable video gains	4 choices over a range of x1 to x9.5
Timing sequencer	DSP56002, 40 nsec per instruction, 50 MHz clock
On board Memory	32k x 24 bits; 8k P: program, 8k X: data and 16k Y: data memory Memory loaded either from on-board EEPROM or over fiber optic link from the host computer
Clock drivers	24 drivers per board; range of each is -10 to +10 V in 0.01 V steps Drive current is 60 mA, with a rise time of 20 nanosec (10 volt step)

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