CCD controller requirements for ground-based optical astronomy

Robert Leach

Dept. of Astronomy, San Diego State University
San Diego CA 92182 e-mail: leach@mintaka.sdsu.edu

ABSTRACT

Astronomical CCD controllers are being called upon to operate a wide variety of CCDs in a range of ground-based astronomical applications. These include operation of several CCDs in the same focal plane (mosaics), simultaneous readout from two or four corners of the same CCD (multiple readout), readout of only a small region or number of regions of a single CCD (sub-image or region of interest readout), continuous readout of devices for drift scan observations, differential imaging for low contrast polarimetric or spectroscopic observations and very fast readout of small devices for wavefront sensing in adaptive optics systems. These applications all require that the controller electronics not contribute significantly to the readout noise of the CCD, that the dynamic range of the CCD be fully sampled (except for wavefront sensors), that the CCD be read out as quickly as possible from one or more readout ports, and that considerable flexibility in readout modes (binning, skipping and signal sampling) and device format exist. A further requirement imposed by some institutions is that a single controller design be used for all their CCD instruments to minimize maintenance and development efforts. A controller design recently upgraded to meet these requirements is reviewed. It uses a sequencer built with a programmable DSP to provide user flexibility combined with fast 16-bit A/D converters on a programmable video processor chain to provide either fast or slow readouts.

Keywords: CCDs, optical astronomy

1. INTRODUCTION

Most early astronomical CCD cameras implemented nearly two decades ago were used for direct imaging applications, and broad-band filters were often used with fairly long exposure times so the high sky and object photon fluxes resulted in enough detected photons that their Poisson counting noise dominated the high readout noise of early CCD devices[1,2]. Early CCDs had only a single readout circuit because their small area made the image readout time acceptable for most applications, and most instruments contained only a single CCD because of the difficulty and expense of acquiring good quality CCDs. In these cameras a simple readout protocol was utilized: at the end of the exposure the charge from each CCD pixel was transferred in sequence to the readout circuitry, whose output numbers were displayed and analyzed in the same geometry as CCD image plane. The flexibility of these cameras was generally limited to having jumpers that could be set to the number of rows and columns to be read out so they could be used with different format sensors. These cameras contained a controller that consisted of the circuits to drive the CCD clocks, a video processor, an analog-to-digital (A/D) converter and a digital waveform generator (or sequencer), and were typically implemented with simple digital logic circuits, often on hand-wired boards that were expensive to duplicate.

With the success of these early cameras in ground-based astronomical observations and the improved performance of available CCDs in the late ’70s and early ’80s came a proliferation of instruments with CCDs detectors and a parallel invention of several innovative operating modes to address a diversity of observational requirements. These included spectrographs[3], drift scanning direct imagers [4,5], differential imagers for polarimetry [6], the operation of multiple CCDs in a single focal plane (mosaics)[7], and star trackers[8]. To operate CCDs in these modes several controllers were designed that were programmable to varying degrees, the most versatile ones typified by Marcus, et. al.[9] and Jorden, et al.[10]. More recent innovations have been the implementation of several readout circuits on a single CCD[11] and the use of CCDs as wavefront sensors in adaptive optics systems[12]. In section 2. below each of these operational modes will be described in more detail to illustrate the way in which the CCDs can be controlled.

Parallel to this evolution of CCD operational modes has been an evolution in the performance of CCD sensors in the astronomical important areas of readout noise, readout speed and number of pixels per device. Other areas of CCD performance of importance to astronomical applications such as dark current, quantum efficiency and charge transfer efficiency that have little bearing on controller performance will not be discussed. The readout noise of CCDs has declined markedly over the years, and recent announcements indicate low readout noise at fast readout speeds have been achieved. There has also been a dramatic increase in the number of pixels per CCD from of order 10^4 twenty years ago to of order 10^7 now. These three parameters place new demands on controllers operating recently developed astronomical CCDs, especially if they are to operate in a diversity of operational modes.

2. ASTRONOMICAL CCD READOUT MODES

Perhaps the simplest variation on simple whole image readout is drift scan[4,5]. The scene to be observed is allowed to drift across the image plane of the CCD while each line of the CCD is clocked at the same rate at which the image is drifting. Typically the telescope tracking is just turned off and the image is read out at the sidereal rate. Every pixel in a given column detects light and contributes to the final image, so variation in the pixel-to-pixel sensitivity are smoothed out, rendering flat-field corrections simpler and more accurate. The controller required for this readout is just a bit more sophisticated - the command to read a line needs to be synchronized to an external clock.

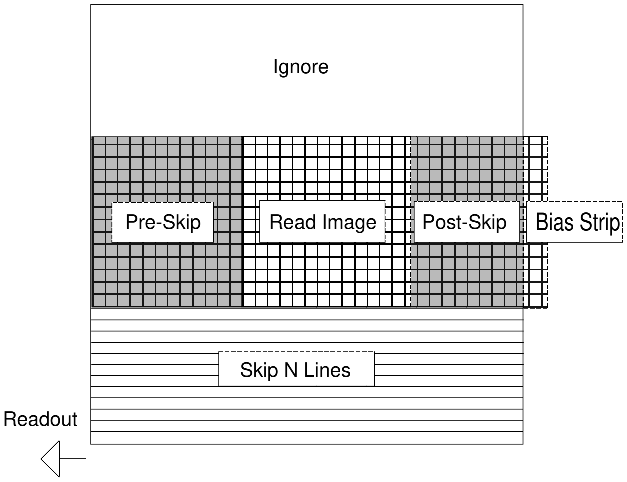

Fig. 1 - Sub-image readout with bias stripe. The readout direction is to the bottom and left to the lower left hand corner. All but the 'Read Image' is skipped over.

More sophisticated then drift scan is sub-image readout, wherein only a portion of the CCD is read out, the rest being simply discarded. Fig. 1 shows a cartoon of this process. The portion of the image to be read is shown at the center, and a bias strip for calibration is also shown as needing to be read out. The N lines below the area to be read out can be skipped over very quickly by executing a cycle of parallel clocks for each line. This time is typically a few tens of microseconds compared to a time to read each line of several tens of milliseconds, so a significant readout time decrease results. At the end of skipping the N lines the charge built up in the serial register needs to be cleared out by executing a cycle of serial clocks, one cycle for each column in the CCD. The cycle time for serial clocks is a few hundred nanoseconds for typical astronomical controllers and CCDs, which is much shorter than a typical pixel processing time because the latter includes time for the signal integration and A/D conversion, which is typically several tens of microseconds. Once the readout arrives at a line containing the pixels to be read out, the parallel clocks transfer one line at a time and the number of columns in the pre-skip region shown in the figure are skipped with the fast cycling of serial clocks. The image pixels are then read normally, after which the post-skip pixels are dismissed and the bias pixels are read normally. The top of the image can be ignored as long as there is a fast clearing of the entire CCD before the next exposure begins to remove charge from the entire array. The clearing can be a series of parallel clock cycles.

Variations on the sub-image readout mode have been described for use in star trackers[8], wavefront sensors for adaptive optics work[12] and fast photometers[11,13]. Several or more sub-images are created on the CCD, with all the areas not being read discarded by either serial or parallel clocking. Lines without stellar images are discarded with the fast parallel clocking, whereas lines containing stellar images must be skipped over one pixel at a time. Clearly the demands on a controller for these applications can be considerable depending on the number of stars, the skipping and reading rates desired, whether the location of the stellar image regions changes with time, and whether a line can contain more than one stellar image.

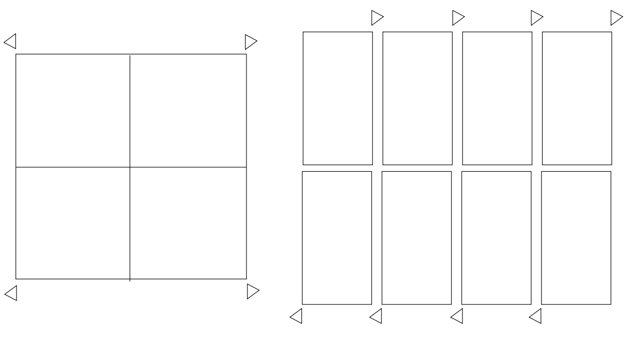
Fig. 3 - Simple schematic of a single CCD with four readouts and a mosaic consisting of eight single readout 2k x 4k CCDs.

Multiple readout CCDs have been manufactured for many years. They are described in a recent context[11], and a review of current mosaic projects was presented by Luppino[15]. The geometry of systems described in these two references is shown in Fig. 3, to dramatize the challenge to controllers. The top of the figure shows the

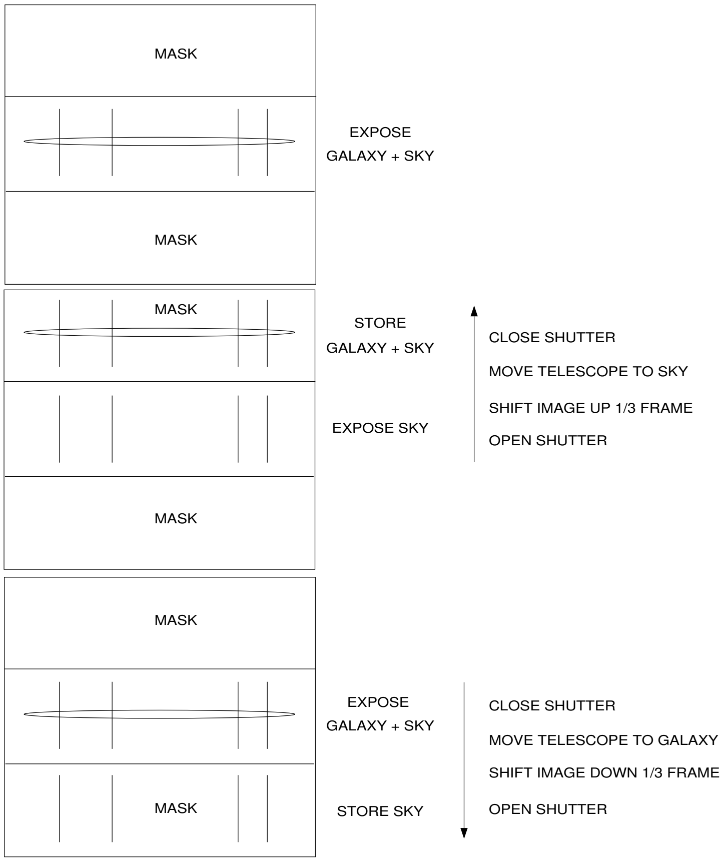

Fig. 2 - Differential imaging sequence for spectroscopy of faint surface brightness objects in the presence of spatially and temporally varying sky background.

arrangement for four readouts on a single CCD, each at a corner. The geometry is a bit simpler for an eight CCD mosaic because there is only one readout per CCD shown. The challenge to controllers is simply to replicate the clock driver and video processor circuits required and to build a fast enough data system to read them out in a timely fashion.

Differential imaging for polarimetric[6] and spectroscopic observations[14] are illustrated Figure 2, which illustrates the spectroscopic mode. The need arises because the sky varies significantly on a time scale of the observation, which may be several tens of minutes long, and multiple images cannot be taken because of the penalty in readout noise and time that is incurred. Additionally, flat-field correction is improved because the same pixels are used for detecting the galaxy plus sky and sky only images. Instead, two types of images are interleaved several times - observations of galaxy plus sky, and of just sky. The two images are stored in the CCD at the same time by employing an optically opaque mask that converts the top and bottom thirds of the CCD into a storage region. The first observation, which may be a few minutes in duration, consists of a galaxy plus sky image in the center. The the shutter is closed, the image is moved to the upper masked region for storage and the telescope is moved to a nearby region away from the galaxy. The shutter is opened to begin a sky only image. After an exposure time equal to the galaxy plus sky the shutter is again closed, the two images are moved down by one third the CCD size so the previous stored galaxy plus sky image is now in the center for additional exposure time and the sky only image is in the bottom masked storage region. The telescope centered on the galaxy, the shutter is opened, closed again and the image moved up so a sky only image is taken. This might be repeated several times before the image is read out in the conventional manner. Polarimetric observations proceed in much the same way except the telescope is kept pointing on the object and the two images are for different senses of a polarization analyzer placed ahead of the CCD. The controller required for this type of readout is not very sophisticated, as the ability to clock parallel register in both forward and reverse directions by a determined number of lines is required.

3. KEY CCD PARAMETERS AFFECTING CONTROLLER DESIGN

The CCDs currently being developed and implemented on ground-based telescopes differ from earlier devices in three important respects that have a bearing on controller design - readout noise, readout time and number of pixels. Pool of the EEV Ltd. company recently reported [16] low readout noise attained with a two stage on-chip preamplifier design developed by Lincoln Labs for CCDs currently in production. He reported 2 electrons rms readout noise at a readout time of 10 µsec per pixel and 3.5 electrons rms at 2 µsec per pixel. These compare to values around 6 electrons rms for readout times of 20 µsec per pixel for the widely used Loral devices and 2-3 electrons rms for SITe operated at extremely long readout times of more than 200 µsec. These devices have a high node sensitivity in the range of 10-20 microvolt per electron, an order of magnitude higher than typical Loral and SITe devices. Also becoming available are ever larger numbers of pixels[15], as 2k x 4k devices are being incorporated in large mosaic cameras, and larger CCDs are under development.

The development of fast low noise amplifiers is important for the practical utilization of CCDs in ground-based astronomy because it sharply reduces the readout time for the large CCDs. A single readout 2k x 4k CCD operated at the conventional readout time of 20 µsec per pixel required to get acceptable readout noise takes about 3 minutes. Operation with the newer low noise devices would reduce this by a factor of ten to 20 seconds, allowing less time to be spent with the shutter closed reading out and more time acquiring photons through the telescope. The challenge for controllers is then to operate these newer CCDs at the speeds that they are capable in multiple readout, programmable controllers that can implement the variety of readout modes that astronomers have devised for their variety of instruments.

4. A NEW CONTROLLER DESIGN

The Dept. of Astronomy at San Diego State developed a CCD controller suitable for astronomical ground-based cameras several years ago that has been distributed to observatories worldwide[17]. We are currently upgrading the design to reflect the improvements in CCDs that have been made in the last several years, especially in the area of readout speed and more efficient operation of multiple readouts. The controllers are expected to become generally available in several months time from the date of this conference. The same general architecture and design philosophy is being employed in the upgrade, and some of the boards will be usable as well. The following sections describe in detail the design of each of the boards of the new design controller boards, except for the computer interface boards for SBus and VMEbus. A table at the end of this section summarizes the expected performance of the upgraded controllers.

4.1 Timing Board - A Motorola DSP56002 monolithic digital signal processor is used as the basic timing generator of the controller. It has a 24-bit data word length, a 16-bit address space, on-chip memory, some communication peripherals and a rich instruction set. It is driven with a 50 MHz clock to give it an instruction processing time of 40 nanosec. The DSP functions as a timing generator by writing 24-bit data words from its internal memory to its data bus every instruction cycle, which are decoded by external circuitry to control various functions. Memory external to the DSP has been implemented with a bank of 32k x 24-bit, no wait state SRAMs, providing 8k additional words of P: program memory, 8k of X: and 16k of Y: data memory.

Communication is implemented between the host computer interface board and the timing board, and between the utility board and the timing board. The utility board controls system functions not directly related to the CCD such as exposure timing, temperature control, shutter operation and power supply control. The host computer interface communicates with the timing board over a fiber optic data link with a scrambled NRZ protocol developed by AT&T that operates from DC to 50 Mbits/sec. A clock recovery chip, jumpered for the desired data rate, supplies a serial data signal and a re-timed synchronous clock to a serial-in parallel-out shift register implemented with a Cypress Semiconductor CY7C372 PAL. The serial word consists of a start bit, 24 data bits, and four stop bits. To protect against noise on the serial data line that occurs especially on power on and off one pattern of stop bits indicates a valid data word, which when received will cause the PAL to assert the fiber optic interrupt request line FOIRQ for the DSP to read the data bits. Another pattern of stop bits indicates that a DSP reset is desired, causing the serial receiver PAL to assert the DSP reset line. This way the controller can be reset remotely from the host computer via software control even if the DSP is not responding to incoming commands. A jumper can be inserted to disable the interpretation of these stop bits if the controller is to be operated with earlier revision host computer interface boards that do not support this feature.

While only commands are received by the timing board both replies and image data are transmitted by the timing board to the host computer interface. Replies are transmitted with the same start bit + 24-bit data + stop bits protocol of the receiver, but image data can be transmitted as start bit + 16-bit data to improve the data link bandwidth. The link operates at 50 MHz, allowing image data to be transmitted in 400 nanosec per pixel, with a 60 nanosec buffer between pixel words. This is a sustained data rate of 2.5 million pixels per second, or 5.0 Mbytes per second, and sets the fastest readout rate for controller systems configured with a large number of readouts. For backwards compatibility image data can also be sent in the 24 bits per pixel format (set by the WW line that the DSP controls) and with or without the stop bits on the reply words. To facilitate transmission of image data from multiple readouts a PAL is used to read image data from the A/D converters on the video processor cards over the backplane, as it asserts address lines ADADR0-5 in sequence to read up to 32 A/Ds. Each A/D value is read by the serial transmitter and sent over the fiber optic link, at the end of which the PAL reads the next A/D value until all of them are read. This sequence of A/D reads and transmissions is initiated with a single DSP command that asserts the line SXMIT and loads in the starting A/D number to read (D0-D4) and the ending number (D5-D9). This feature is implemented to allow CCD timing operations to overlap with the image data transmission.

Communication between the utility and timing boards is implemented over the synchronous serial interface (SSI) implemented on the DSP56002. It is a fast link (3.1 Mbits/sec) that operates with just a clock and data line in a 24-bit per word, on-demand protocol. This same link is used to transmit configuration data to the video processor and clock driver boards, with the serial link decoding being done instead by PALs on the selected board, as discussed below. The bit H0 selects between words being sent to the utility or the analog boards.

The DSP56002 implements an emulator function called the OnCE (On Chip Emulator) via four pins on the DSP. These are brought out to a fourteen pin connector at the edge of the board with a pinout that matches a companion board that Motorola markets for operating from a Sun, Mac or PC. The emulator can be used for a variety of debugging tasks since it allows the DSP to execute code in real time, which can be interrupted by installing breakpoints so the user can examine the contents of all internal registers and memory contents.

There are digital-to-analog converters (DACs) on the clock driver and video processor boards that have their digital voltage value generated by the timing board, usually during controller initialization. The DSP serial synchronous interface (SSI) is used for this, as the 24-bit serial word is routed with a start bit and a continuously running clock to the backplane if the H0 bit of the DSP is set. If H0 is cleared the SSI signals are routed to the utility board. The 24 bits of the serial word are defined as follows -

Serial link bit assignment for writing to DACs:

D23 to D20	D19 to D16	D15 and D14	D13	D12	D11 to D0
board select	select DAC	select circuit in DAC	DAC or MUX	N/U	DAC voltage

The bits D20-D23 select which board to update, based on jumpering on the board. The four bits D16-D19 select which DAC package will be updated on the selected board (with 12 DACs on the clock driver board and four DACs on the video processor board). D14 and D15 select which of four DAC circuits within the selected DAC package is selected for updating with the 12 bits of data D0-D11.

During CCD readout the DSP writes 24-bit data words from its internal memory onto its external bus as often as one word every 40 nanoseconds. The eight most significant bits are interpreted by the timing board as delay bits for inserting wait states of as small as 20 nanoseconds each before the next data word is read and interpreted. The most significant bit D23 selects either a coarse or fine delay mode, wherein coarse delay sets the number D16-D22 of 200 nanosec delay steps, for delays over the range of 0.2 to 25.6 microsec. The fine delay selects the number D16-D23 of 20 nanosec delays, for delays over the range of 20 to 2500 nanosec. The maximum delay of 25.6 microsec was chosen to allow the DSP to service interrupts such as might result from incoming serial data without too much delay since interrupts cannot be processed while the DSP is in a delay mode. The remaining 16 bits are written to the backplane on the lines SS0-SS15 for decoding by the clock driver and video processor boards. The bits SS12-SS15 select which board is operative based on jumpers located on each board, and the 12 remaining bits D0-D11 simultaneously set the state of twelve analog switches only on the selected board. The clock driver board sets the state of half of its clock drivers to one of two DAC values, and uses the least significant bit SS12 of the board select bits to select either the upper or lower half of the sets of twelve clock drivers, since there are a total of 24 on a board.

Parallel word bit assignment for updating switch states:

D23	D22 to D16	SS15 to SS12	SS11 to SS0
coarse or fine delay	delay value	board select	state of each of 12 analog switches

4.2 Video Processor Board - The video processor is designed to read out from low noise astronomical CCDs in either conventional slow speed rates of around 18 µsec/pixel or in a fast readout mode of up to 2 µsec/pixel. It is shown schematically in Fig. 4. It contains a low noise front end preamplifier that is DC coupled to the CCD and contains a DAC controlled input offset adjustment operating at a gain of x5. The preamplifier connects to a post amplifier that has a choice of four software controlled gains over a range of x1 to x10. It is a low impedance driver feeding a pair of amplifiers to select the polarity of the signal input to the integrator, one operated at a gain of -1, one at a gain of +2. The output of both are summed on a Deboo integrator, with the +2 gain switched in only after the CCD charge is dumped onto the output node. A sample/hold and output offset adjustment stage follows with enough output drive current to drive the analog-to-digital converter. The A/D converter is an Analogic part ADC4325 with 16 bits accuracy and a two microsec combined sample-hold and convert time. A/D convert overlaps with all operations of the video processor board, allowing pixel processing times of two microseconds. Two identical video processors are installed on each video processor board for connection to two separate CCD readouts, with a shared PAL on the board for address decoding when reading the A/D digital output values and setting the voltages of the DACs, discussed below.

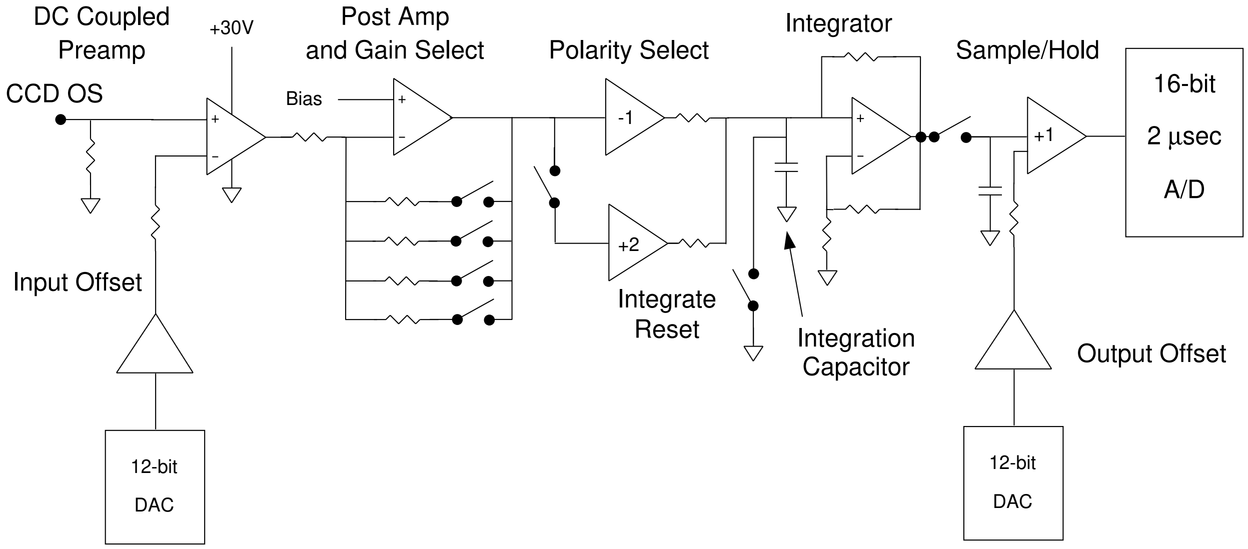

Fig. 4 - Block diagram of video processor

Three DAC packages are provided on each video processor board, for a total of twelve DAC circuits. Four of these are used for the offset circuits (input and output offsets on each of two video processing circuits) and the remaining eight are split four to a CCD for generating low impedance, low noise DC bias supply voltages. One is for the output drain with a range of 0-30 volts, one is for the reset drain with a range of 0-20 volts, one is for the output transfer gate with a range of -5/+5 volts, and one is uncommitted, with a range of -15/+15 volts. Similar to the clock driver board MOSFET switches are placed between the DC bias supply drivers and the board output to disconnect the supplies from the CCD until they are fully configured during power up, or to disconnect them suddenly if there's a power failure.Either the power control board,
the utility board or the timing board can turn the MOSFET switches off.

4.3 Clock Driver Board - The clock driver board generates 24 clocked signals over the range of -10 to +10 volts for driving CCD registers directly. Several clock driver boards may be installed in a single controller system for driving mosaics of CCDs or CCDs with complex architectures, or both. The clocks are generated by analog switches selecting from one of two voltages determined by DACs, whereby up to twelve switch states on a clock driver can be changed in a single 40 nanosec instruction cycle. The DAC voltages are updated over the serial link from the timing board, taking about 2 µsec per voltage. Each DAC package contains four DAC circuits, and drives two CCD clocks.

A single large Cypress PAL interprets and decodes the serial data used to update the DAC voltages according to the bit assignment discussed above for the timing board. The serial data and clock lines are received as 24-bit words by a PAL that compares the upper bits D20-D23 to the jumper setting on the board. If they match then the PAL examines the DAC select bits D16-D19 to select which of the twelve load lines are to be asserted, each one routed to one DAC package. The DAC addressing bits and voltage values D0-D15 are passed along unchanged to all the DACs on the board, but only one of the four internal DACs of the DAC package selected by the FSYNC signal is updated. A global control signal generated by the timing board runs to all the clock driver boards to clear the contents of all the DACs prior to programming.

Each DAC output is passed through a low pass filter and connected to a SPST analog switch. A pair of DAC outputs are connected to a pair of analog switch inputs that are configured with one switch being normally open and the other one normally closed. The switch state is controlled by the data bits D0-D11 written by the timing board over the backplane every instructions cycle. Four of the data bits (D12-D15) are board select bits that map into a fast 22V10 PAL that is programmed as a comparator between the bits an a set of four jumpers. If the comparison passes the data bits are latched onto one of two sets of latches, depending on the value of D13. The two outputs of the analog switch are connected together so one of the two DACs is always selected, and is input to a driver op amp. The op amp was selected for high drive current (60 mA), high speed (2000V/µsec), low noise (2 nV/√Hz) and low power consumption (6.5 mA). Finally, the clock signals are passed through a low resistance MOSFET switch so the clocks can all be turned off with a global signal from the timing board prior to initialization or if the power gets corrupted.

Several multiplexers connect selected clock driver output pins to coaxial connectors for use during debug and setup. Two independent multiplexers allow two clock signals to be monitored simultaneously so clock signal overlap when driving the CCD can be examined. Several regulator circuits provide +/- 12 volts for the DACs, op amps, MUXes, and analog switches, and -5 volts for the analog switches.

4.4 Utility and Power Control Boards - These boards have been described in detail elsewhere and will remain essentially unchanged in the new design. The utility board provides controller functions not directly involved in the readout, such as exposure timing, shutter control, CCD temperature control, power monitoring, and power turn on. It has many non-dedicated analog and digital inputs and outputs that the user can customize. It operates from an interrupt service routine that executes every millisecond, with the DSP using a small fraction of its processing speed for the programmed functions. The power control board contains three switches to turn on the analog power supplies +15, -15 and +32 volts from the incoming power supply cable onto the backplane where it is distributed to the video processor and clock driver boards. It turns on the power with a linear ramp lasting several tens of milliseconds on command from the utility board in order to avoid power glitches from passing to the CCD that might occur with an sudden or uncontrolled power surge. It also has voltage comparators monitoring the power supply voltages to turn off the supplies if the voltages fall outside allowable limits.

4.5 Performance summary

Typical readout time	18 µsec/pixel
Fastest readout time	2.0 µsec/pixel, limited by A/D converter speed
	3.2 µsec for N = 8 readouts, limited by fiber optic speed
Board size	All boards 10 x 23 cm
Estimated power dissipation	50 watts for 8 readouts
Boards needed for 8 readouts	9
Practical maximum of readouts	16
Computer interfaces supported	VME, SBus
A/D converter	16-bits, 2 µsec/pixel
Selectable gain	4 choices over a range of x1 to x10
Timing sequencer	DSP56002, 40 nsec per instruction, 50 MHz clock
On boardmMemory	32k x 24 bits; 8k P: program, 8k X: data and 16k Y: data memory
CCD clock drivers	24 drivers per board; range of each is -10 to +10 V in 0.01 V steps

5. REFERENCES

1. Young, P., Westphal, J. A., Kristian, J., Wilson, C.P. and Landauer, F. P., "Evidence for a Supermassive Object in the Nucleus of the Galaxy M87 from SIT and CCD Area Photometry," *Ap. J.*, **221**, 721 (1978).

2. Leach, R. W., Schild, R. E., Gursky, H., Madejski, G. M., Schwartz, D. A. and Weekes, T. C., "Description, Performance and Calibration of a Charge-Coupled-Device Camera," *PASP* 92, 233 (1980).

3. Goad, L. E., "Application of a Charge-Coupled Device (CCD) Detector for Coude Spectroscopy," *SPIE Proc.* 331, 130 (1982).

4. McGraw, J. T., Angel, J. R. P., and Sargent, T. A., "A CCD Transit-telescope Survey for Galactic and Extragalactic Variability and Polarizaion," *SPIE Proc.* 264, 20 (1980).

5. Mackay, C. D., "Drift Scan Observations with a Charge-Coupled Device (CCD)," *SPIE Proc.* 331, 146 (1982).

6. Stockman, H. S., "Differential Imaging using Charge-Coupled-Device (CCD) Imagers with On-chip Charge Storage," *SPIE Proc.* 331, 76 (1982).

7. Lockhart, R. F., "Wide Field and Planetary Camera for Space Telescope," *SPIE Proc.* 331, 388 (1982).

8. Stanton, R. H., Alexander, J. W., Dennison, E. W., Glavich, T. A. and Hovland, L. F., "Optical Tracking Using Charge-Coupled Devices," Optical Engineering 26, 930 (1987).

9. Marcus, S., Nelson, R., and Lynds, R., "Preliminary Evaluation of a Fairchild CCD-211 and a New Camera System," SPIE Proc. 172, 207 (1979).

10. Jorden, P. R., Thorne, D. J. and van Breda, I. G., "Royal Greenwich Observatory (RGO) Charge-Coupled Device (CCD) Camera," *SPIE Proc.* 331, 87 (1982).

11. Leach, R. W. "Noise and Readout Performance of a Multiple-Readout CCD Controller," SPIE Proc. 2198, 821 (1994).

12. Beckers, J. M., "Adaptive Optics for Astronomy: Principles, Performance and Applications," Ann. Rev. of Astr. and Ap., 31 (1993).

13. Abbott, T. M. C. and Opal, C. B., in Instrumentation for Ground-Based Optical Astronomy: Presetn and Future," ed. Robinson, L. B., pg. 386, Springer-Verlag, New York, 1988.

14. Sembach, K. and Tonry, J., "Ultra-Low Surface Brightness Spectroscopy of Elliptical Galaxies," Bull. AAS 27, 1408 (1996).

15. Luppino, G. A. "Design of an 8192 x 8192 pixel CCD mosaic," SPIE Proc. 2198, 810 (1994).

16. Pool, P. from Laser Focus World, Jan. 1996, as presented in Sci. Opt. Imag., Georgetown, Grand Cayman.

17. Leach, R. W., "Optical Astronomy from the Earth and Moon,", Eds. Pyper, D.M. and Angione, R. J., ASP Conf. Series #55, 113, (1994).