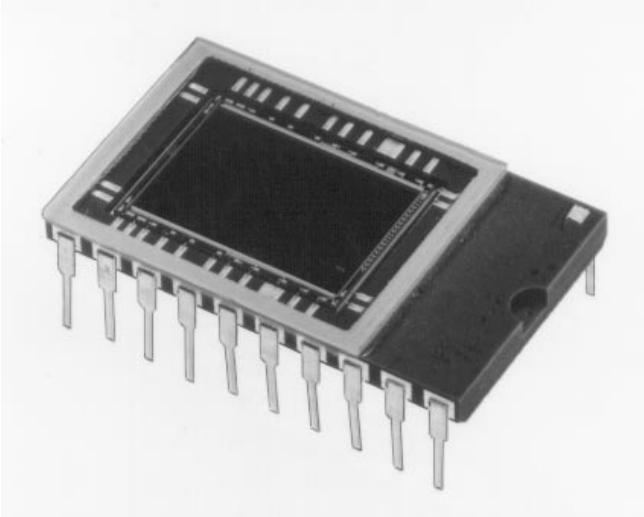
CCD02-06 Deep Depletion Sensor
High Performance CCD Sensor

FEATURES

- 385 (H) by 578 (V) Pixel Format
- 22 µm Square Pixels
- Active Area 12.7 x 8.5 mm
- Low Pixel Readout Noise
- Enhanced Infrared (IR) Sensitivity
- Uniform Response over Whole Image Area
- High Charge Transfer Efficiency
- Wide Dynamic Range
- Radiation Tolerant



APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation

INTRODUCTION

The CCD02-06 series deep depletion sensor has a 385 x 578 pixel format, each pixel being 22 µm square. Devices feature very low noise operation at cryogenic temperatures and are available in three quality grades.

The deep depletion variant of the CCD02-06 has much improved infrared sensitivity. It is pin and clock compatible with the standard CCD02-06.

The image sensing area of 12.7 x 8.5 mm is intended for use in the full-frame method of operation, either in slow scan mode or in time delay integration mode with final readout through the on-chip register and output amplifier. Signals are usually fed to a framestore or computer for processing and reformatting for display purposes.

Standard three-phase clocking and buried channel charge transfer are employed.

The CCD02-06 deep depletion sensor is primarily intended to suit the requirements of astronomy and scientific measuring instruments but is suitable for use by other specialist users in applications requiring precise image analysis measurements over a very wide dynamic range.

Further information on deep depletion CCDs can be found in EEV CCD Technical Note 101.

TYPICAL PERFORMANCE

Pixel readout frequency	20 - 3000	kHz
Output amplifier sensitivity	1.0	$\mu V/e^-$
Peak signal	300	ke^-/pixel
Dynamic range	37 500:1	
Spectral range	420 - 1080	nm
Readout noise (at 253 K, 20 kHz)	8	e^- rms
QE at 700 nm	45	%
QE at 850 nm	47	%
Peak output voltage (unbinned)	300	mV

GENERAL DATA

Format

Image region (section A)	385(H) x 288	pixels
Image region (section B)	385(H) x 290	pixels
Image area (sections A + B)	12.7 x 8.5	mm
Pixel pitch (row and column)	22 x 22	µm

Package

Package size	25.4 x 15 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Inter-row spacing	15.24 mm
Window material	quartz or removable glass

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	100k	300k	-	e^-/pixel
Peak output voltage (unbinned)	-	300	-	mV
Dark signal at 293 K (see note 2)	-	60k	120k	e^-/pixel/s
Charge transfer efficiency (see note 3):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier sensitivity	0.6	1.0	1.4	$\mu V/e^-$
Readout noise at 253 K (see note 4)	-	8	10	rms e^-
Readout frequency (see note 5)	-	20	3000	kHz
Response non-uniformity (std. deviation)	-	3	-	% of mean
Dark signal non-uniformity at 293 K (std. deviation)	-	6k	12k	e^-/pixel/s
Output node capacity relative to image section	-	3.0	-	

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level):

	Min	Typical	Max	
I∅/I∅ interphase	-	3.0	-	nF
R∅/R∅ interphase	-	40	-	pF
I∅/SS	-	10	-	nF
R∅/SS	-	70	-	pF
Output impedance	-	1.5	-	kΩ

NOTES

1. Signal level at which resolution begins to degrade.
2. Measured between 233 and 253 K and at V_{SS} +9.0 V. Dark signal at any temperature T (kelvin) may be estimated from:
   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
   where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices.
3. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
4. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 µs integration period.
5. Readout above 3000 kHz can be achieved but performance to the parameters given cannot be guaranteed.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a responsivity of less than 90% of the local mean signal illuminated at approximately half saturation.

White spots Are counted when they have a generation rate 10 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 253 K). The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by:
$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

White column A column which contains at least 9 white defects.

Black column A column which contains at least 9 black defects.

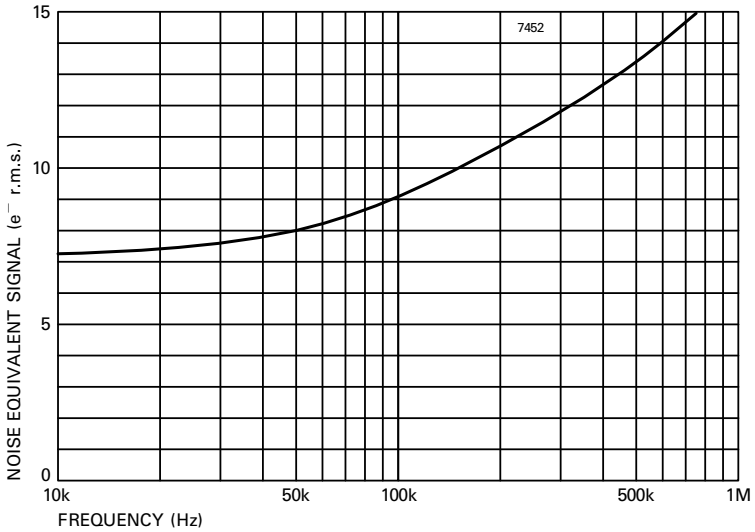
GRADE	0	1	2
Column defects:			
black or slipped	0	1	3
white	0	0	0
Black spots	4	6	80
Traps >200 e^-	0	1	5
White spots	10	10	15

Minimum separation between adjacent black columns . . . . . 50 pixels

Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

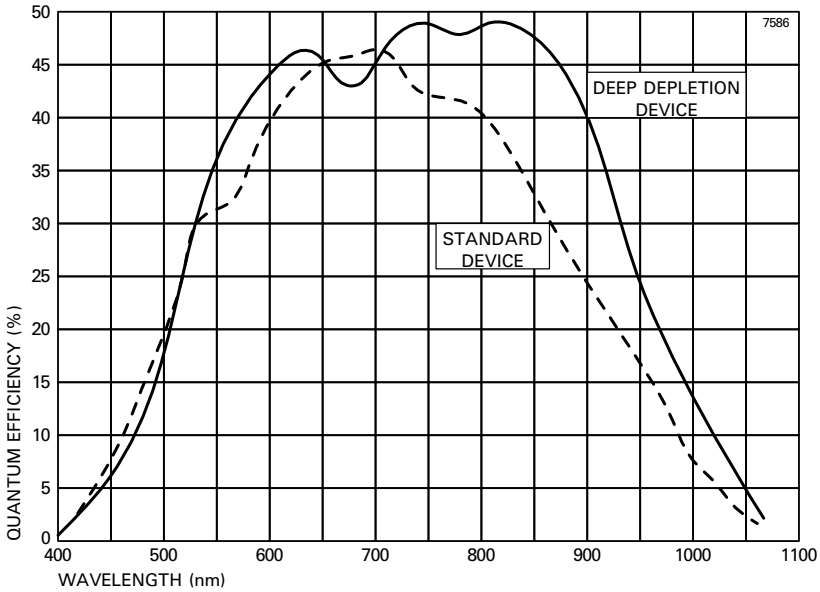
TYPICAL OUTPUT CIRCUIT NOISE

(Measured using clamp and sample)

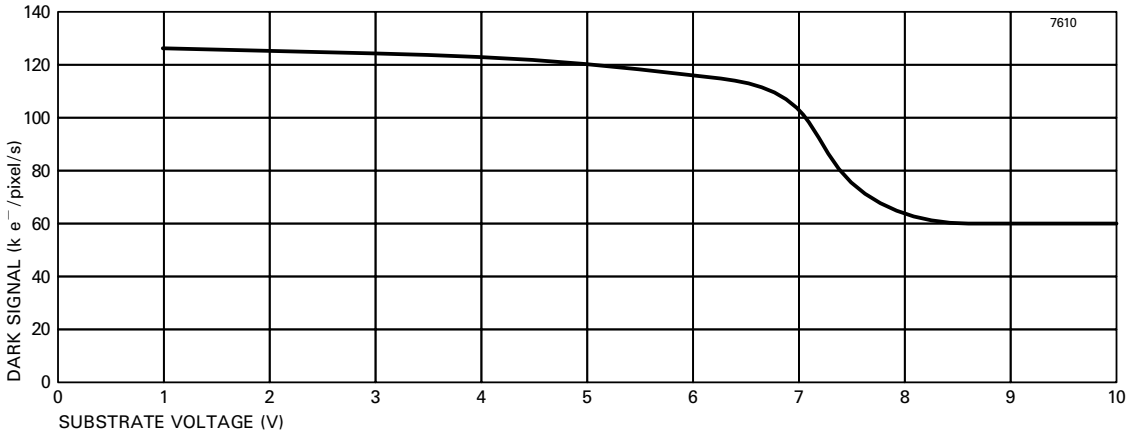


TYPICAL SPECTRAL RESPONSE AT 20 °C

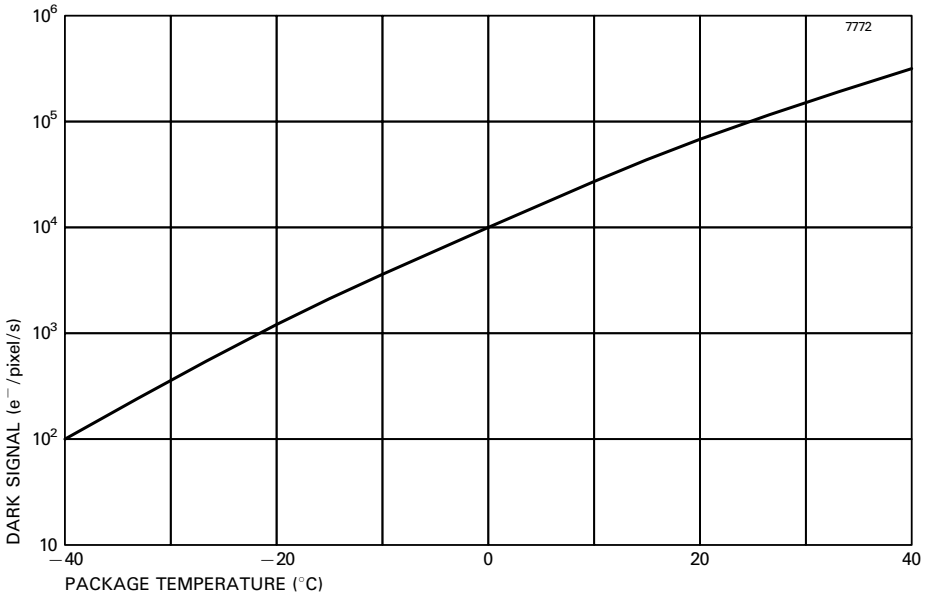
(No window)



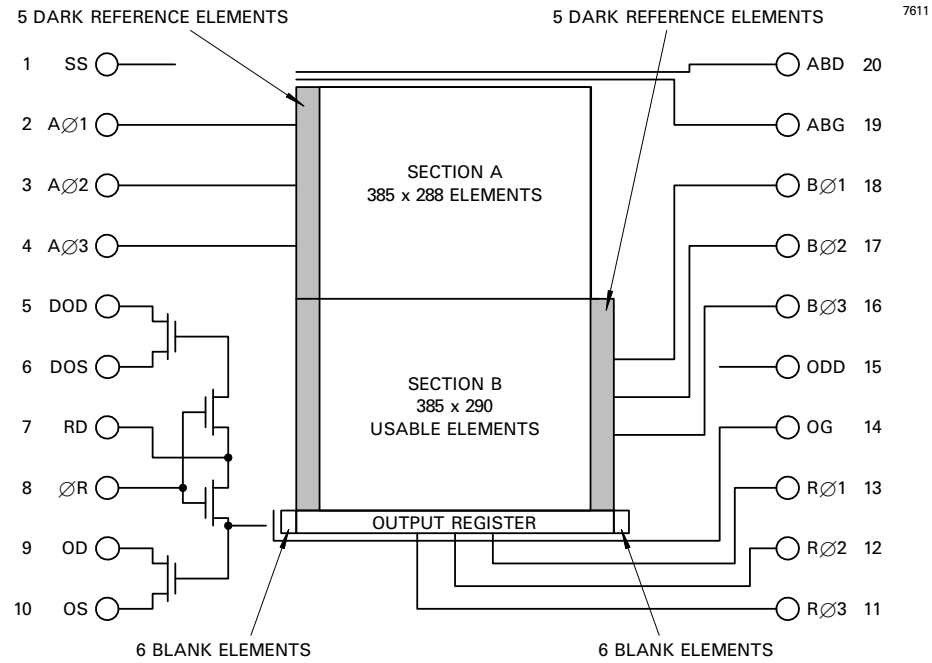
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE (At +20 °C)



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



For device operation in the full-frame mode:

IØ1 = AØ1 + BØ1
IØ2 = AØ2 + BØ2
IØ3 = AØ3 + BØ3

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

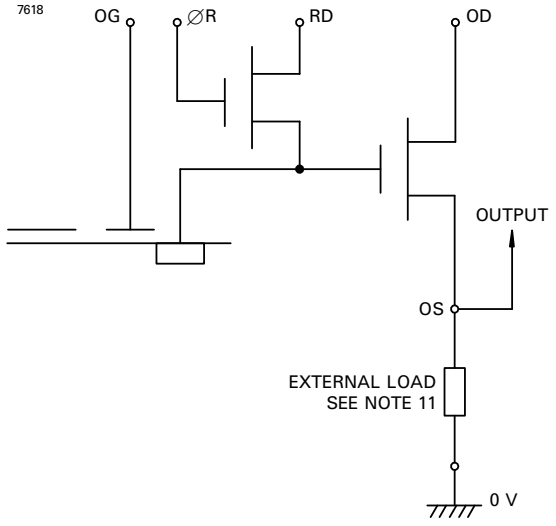
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SS	Substrate (see note 7)	0	9	10	-
2	A∅1	Section A drive pulse, phase 1	8	10	15	±20 V
3	A∅2	Section A drive pulse, phase 2	8	10	15	±20 V
4	A∅3	Section A drive pulse, phase 3	8	10	15	±20 V
5	DOD	Dummy transistor drain (see note 8)	24	V_{OD}	30	−0.3 to +25 V
6	DOS	Dummy transistor source		see note 9		−0.3 to +25 V
7	RD	Reset transistor drain	17	18	19	−0.3 to +25 V
8	∅R	Output reset pulse	8	10	15	±20 V
9	OD	Output drain (see note 8)	27	29	32	−0.3 to +25 V
10	OS	Output transistor source		see output circuit		−0.3 to +25 V
11	R∅3	Readout register, phase 3 (clock pulse)	8	10	15	±20 V
12	R∅2	Readout register, phase 2 (clock pulse)	8	10	15	±20 V
13	R∅1	Readout register, phase 1 (clock pulse)	8	10	15	±20 V
14	OG	Output gate	1	3	5	±20 V
15	ODD	Bias point (see note 8)	24	V_{OD}	30	−0.3 to +25 V
16	B∅3	Section B drive pulse, phase 3	8	10	15	±20 V
17	B∅2	Section B drive pulse, phase 2	8	10	15	±20 V
18	B∅1	Section B drive pulse, phase 1	8	10	15	±20 V
19	ABG	Anti-blooming gate		see note 10		±20 V
20	ABD	Anti-blooming drain		see note 9		−0.3 to +25 V

If all voltages are set to the 'typical' values, operation at or close to specification should be obtained. Some adjustment within the minimum - maximum range specified may be required to optimise performance.

Voltage between pairs of pins: OS to OD ± 15 V.

Maximum current through any source or drain pin: 10 mA.

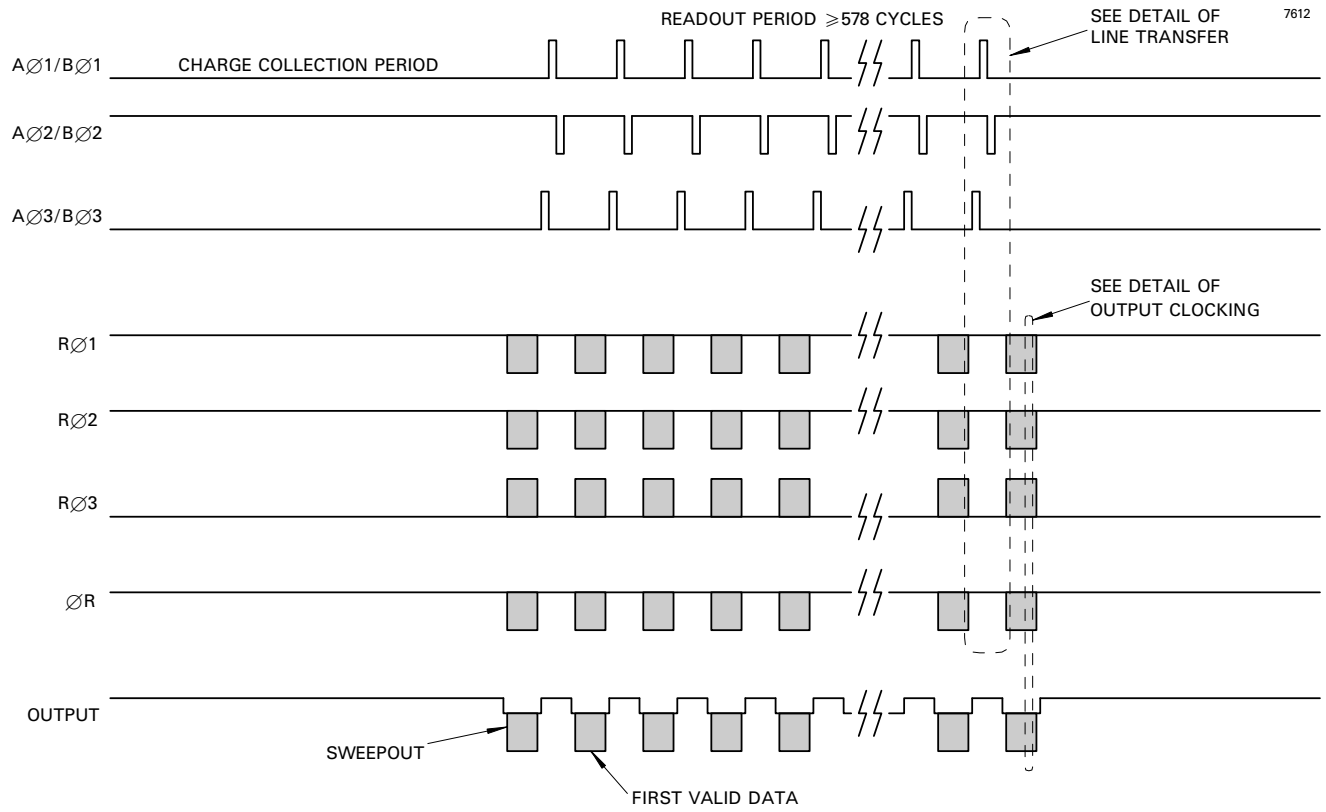
OUTPUT CIRCUIT



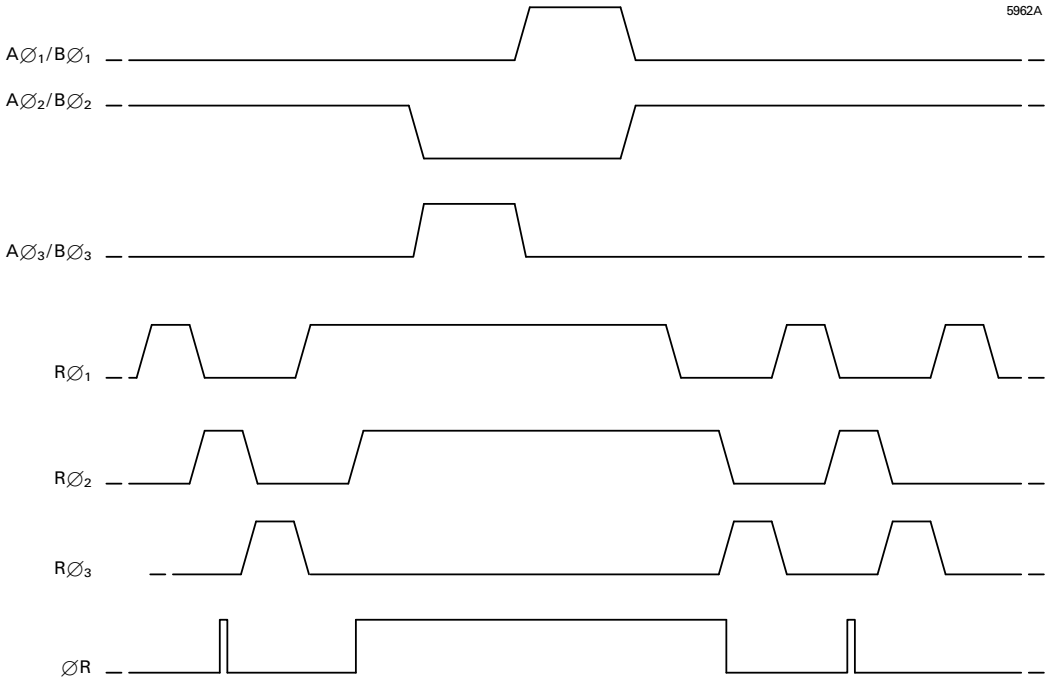
NOTES

6. All image low levels 0 ± 0.5 V. Other pulse low levels +1 V.
7. A 9 V substrate voltage should give minimum dark current. However, for optimum depletion depth (and hence resolution in the infrared) lower substrate voltages should be used.
8. Maximum voltage with respect to substrate 25 V.
9. Not used. Connect to V_{OD}.
10. Not used. Connect to 0 V.
11. Not critical; can be a 1 - 2 mA constant current source, or 15 - 25 kΩ resistor.

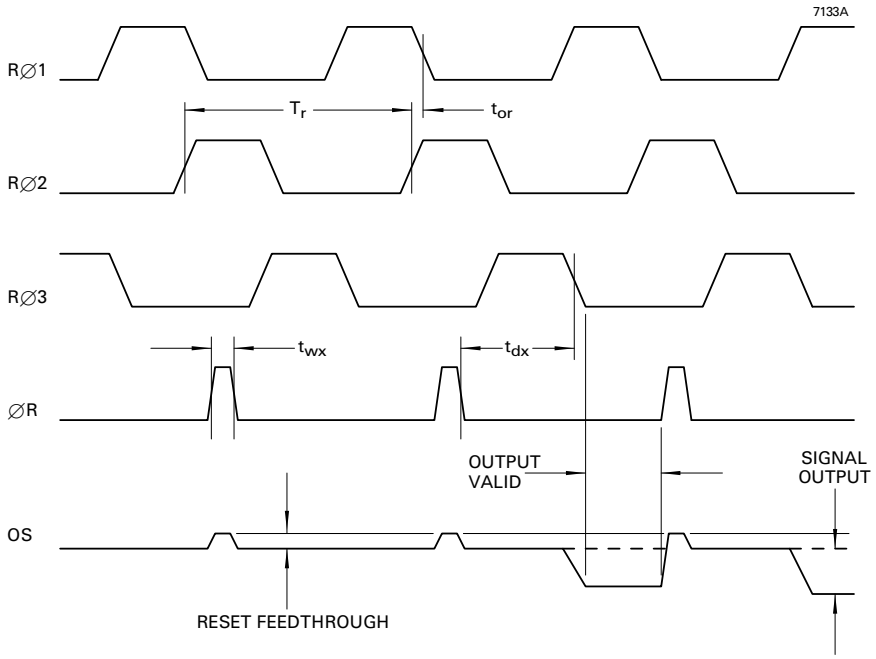
FRAME READOUT TIMING DIAGRAM



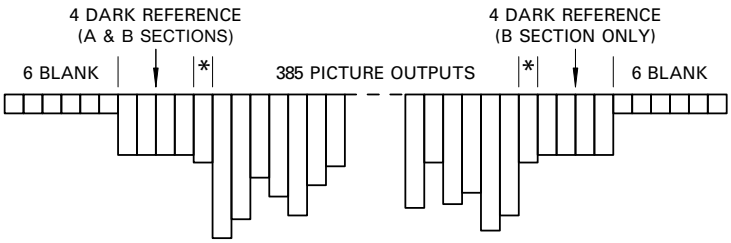
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* Partially shielded transition elements

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CLOCK TIMING REQUIREMENTS

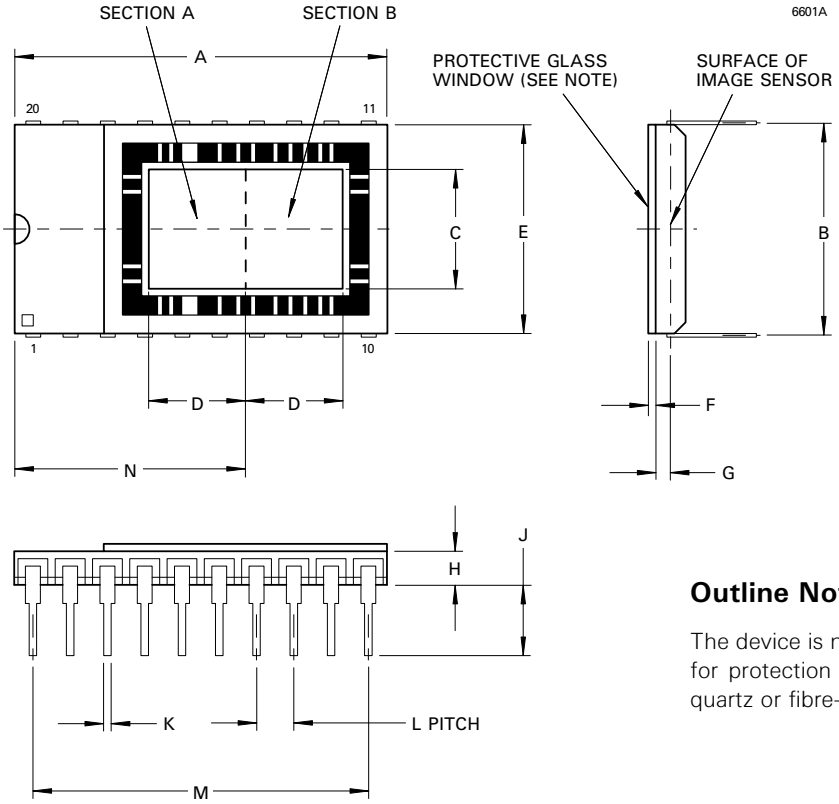
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	5	10	see note 12	µs
t_{wi}	Image clock pulse width	3	5	see note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	1	3	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	1	3	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	5	see note 12	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 12	µs
T_r	Output register clock cycle period	200	see note 13	see note 12	ns
t_{rr}	Clock pulse rise time (10 to 90%)	100	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	40	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
13. As set by the readout period.

OUTLINE

(All dimensions without limits are nominal)



Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

Ref	Millimetres
A	25.40 ± 0.25
B	15.24
C	8.5
D	6.3
E	14.99 ± 0.20
F	0.55 ± 0.10
G	0.70 ± 0.15
H	2.29 ± 0.23
J	5.0
K	0.46
L	2.54
M	22.86
N	15.85 ± 0.25

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window

For further information on the performance of these and other options, please contact EEV.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to greater than 10^4 rads. This corresponds to:

10^{13} of 15 MeV neutrons/cm^2
2 x 10^{13} of 1 MeV gamma/cm^2
4 x 10^{11} of ionising particles/cm^2

Certain characterisation data are held at EEV. Users planning to use CCDs in a high radiation environment are advised to contact EEV.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling	5		K/min