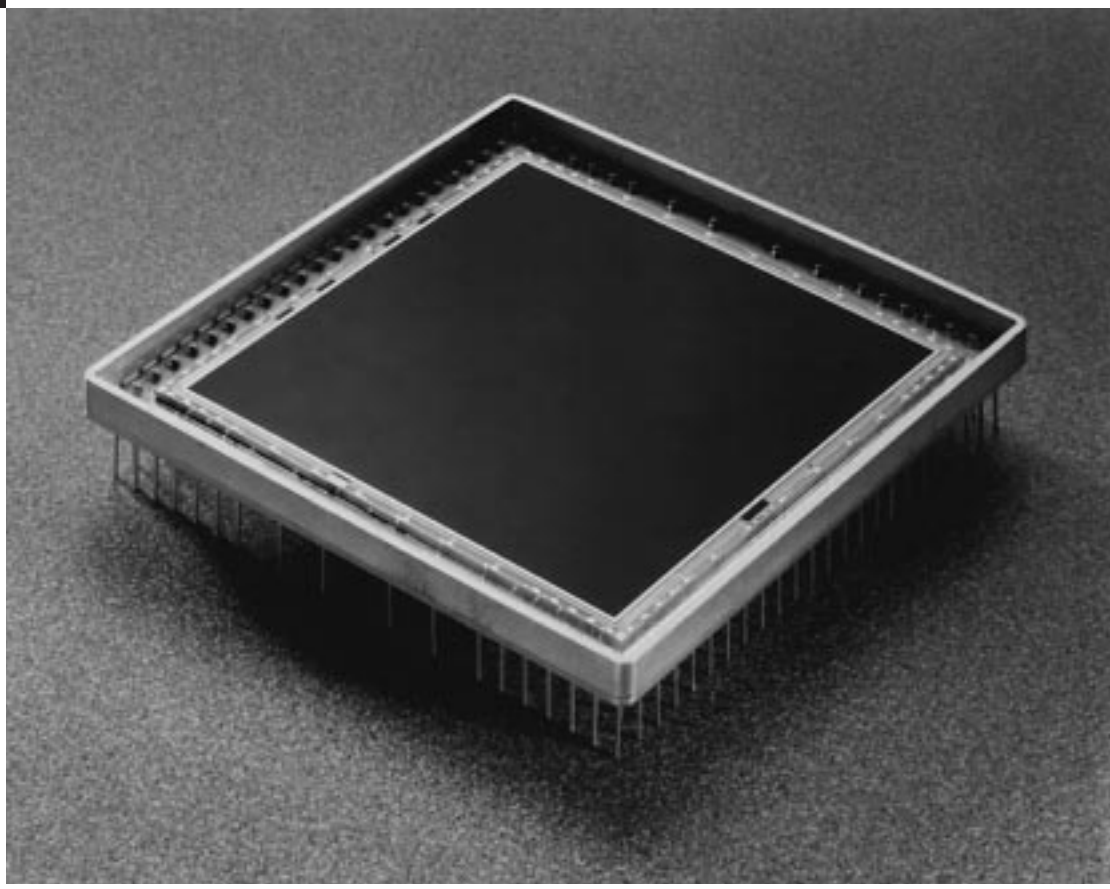


2048 x 2048 pixel format
(24µm square)

■

Front-illuminated or thinned,
back-illuminated versions

■

Unique thinning and Quantum
Efficiency enhancement processes

■

Excellent QE from IR to UV

■

Anti-reflection coating
for visible region

■

Mechanical Rigidity

■

MPP technology

■

Low dark current

■

Ultra-low Dark Current

■

Excellent charge transfer efficiency
(CTE) at all signal levels

■

On-chip output MOSFET
for low noise

■

Wide dynamic range

■

Serial-parallel-serial architecture
with output MOSFETs in each
quadrant for maximized
readout flexibility

■

Applications include astronomy, machine
vision, medical imaging, X-ray imaging,
and scientific imaging

SITe 2048 x 2048 Scientific-Grade CCD

SI-424A CCD Imager: *Ideal for applications with medium-area imaging requirements*

General Description

The SI-424A CCD Imager is a silicon charge-coupled device designed to efficiently image scenes at low light levels from UV to near infrared. The sensor is fabricated as a 2048 x 2048 pixel, full frame area imager that utilizes a buried channel, three level polysilicon gate process. Features include a buried channel with a mini-channel for high transfer efficiency, multi-phase pinned (MPP) operation for low dark current, and lightly doped drain (LDD) output amplifiers for low read noise. The device is available in a front illuminated version or a thinned, back-illuminated version that provides superior quantum efficiency.

SITe's unique thinning and back surface enhancement process provides increased blue and UV response in a flat and fully supported die. The CCD imager is mounted in a non-hermetic metal package without a window.

Functional Description

Imaging Area

As shown in the functional diagram, Figure 3, the imaging area of the SI-424A consists of 2048 columns, each of which contains 2049 picture elements (pixels). Each pixel measures 24µm x 24µm. The columns are isolated from each other by channel-stop regions. The 2049

rows of pixels are further divided into two groups of 1025 rows (upper section) and 1024 rows (lower section) for clocking flexibility and output amplifier selection. There is an output amplifier at each corner of the device, at each end of the two output serial registers. By proper phasing of the parallel and serial clocks any or all of the four amplifiers may be selected.

The signal charge collected in the imaging array is transferred along the columns, one row at a time, to one or both of the serial registers and from there to the desired output amplifiers. The serial registers are also divided into two sections. Thus the array can be divided into quadrants to maximize data transfer rate. The four quadrants are designated by the letters a,b,c,d, corresponding to the nearest output amplifier.

Three levels of polysilicon are used to fabricate the three gate electrodes which form the basic CCD cell (pixel). All of the pixels in a given row are defined by the same three gates. Corresponding gates in each row within a group of 1024 or 1025 are connected in parallel at both edges of the array. The clock signals used to drive the imaging area gates are brought in from both edges of the array, thus increasing the rate at which the rows can be shifted. The two sections of the imaging area are bussed independently for phases 1 and 2, but the phase 3 bus is common to both sections.

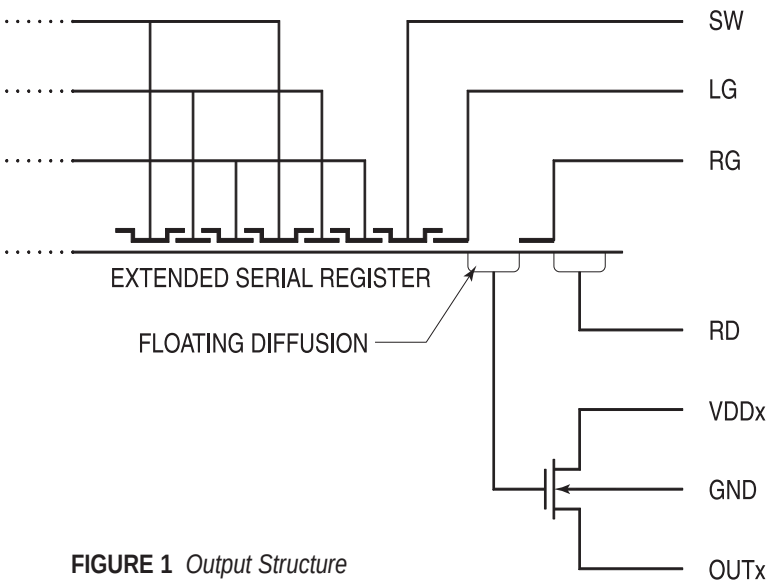


FIGURE 1 *Output Structure*

Serial Registers

The functional diagram (Figure 3) illustrates the relationship between the imaging array and the serial registers. The charge collected in the imaging section is transferred through the transfer gate into the serial register phase 2 gate. The serial register has one pixel for each column in the imaging array, plus 20 extra pixels at each end for a total of 2088. The extra pixels serve as dark reference and ensure that the signal chain is stabilized when the image data is received at the output.

The output of each end of both serial registers is terminated in a summing well, a DC-biased last gate (which serves to decouple the serial clock pulses from the output node), and an output amplifier. The summing well is a separately clocked gate equal in charge capacity to the other serial gates. It can be used to provide on-chip (noiseless) charge summing of consecutive serial pixels. Similarly, it is possible to sum pixels into the serial register by performing repetitive parallel transfers with the serial clocks fixed. In this manner, it is possible to collect and detect as one pixel the sum of the charge in sub-arrays of the imaging section, provided that the sum is less than the full well charge. The well capacity of a pixel in the serial register is greater than that of a parallel pixel to ensure that the CTE remains high.

The two sections of the serial registers are bussed separately for phases 1 and 3, but the phase 2 bus is common to both sections within each serial register. As a result, S2ab and S2cd are driven by a common phase 2 clock for each specific register.

This architecture permits images to be read out of any one or all of the four output amplifiers in a variety of ways. Four major options are represented in the CCD timing diagrams and are described in a later section.

Output Structure

The imager has four output MOSFETs that are located in each corner of the device at the ends of the extended serial registers. Figure 1 presents a schematic diagram of each output configuration.

In operation, a positive pulse is applied to the reset gate (RGx). This sets the potential of the floating diffusion to the potential applied to the reset transistor drain (RDx). The reset gate voltage is then turned off and the output node (the floating diffusion) is isolated from the rest of the circuit. Charge from the serial pixel is then transferred to the output node on the falling edge of the summing well (SWx) clock signal. The addition of charge on the output node causes a change in the voltage on the gate of the output MOSFET. This change in voltage is sensed at OUTx.

Timing

The SITe SI-424A CCD Imager can be operated with one, two, three or four outputs operating simultaneously. The serial gates are separated into left and right halves. Similarly, the parallel gates are separated into upper and lower halves. The quadrants thus formed are designated a (upper left), b (upper right), c (lower left), and d (lower right). See Figure 3.

When operated in the full frame mode, the entire imager's signal is transferred to one output, and all of the same numbered phases of the selected serial register are clocked together. For example, S1c and S1d would be wired together. Likewise, in the parallel registers, P1a, P1b, P1c and P1d would all be wired and clocked together. The signal charge may be clocked out of any output; however, the timing must be appropriate for that output. The transfer gate (TG) adjacent to the chosen serial register must be clocked. The other transfer gate should be held low to prevent unwanted charge in the unused serial register from entering the parallel register.

The unused serial register's gates could be either clocked or held at the proper dc level.

The SI-424A may also be operated in the quad mode wherein the signal charge is clocked out of all four outputs simultaneously. The charge in each quadrant is transferred to the nearest output. The gates in each quadrant are given clocking signals appropriate for full frame operation of that output. For example, S1a, S2ab, S3a and SWa would be clocked according to OUTa timing, and S1a, S2ab, S3b and SWb would be clocked according to OUTb timing. Likewise, the parallels, P1a, P1b, P2a, P2b, P3a, P3b, TGa and TGb should all be clocked according to OUTa and OUTb parallel timing, and the lower half parallel and serial clocks would be clocked according to OUTc and OUTd timing.

Finally, the SI-424A may be operated with two simultaneous outputs by splitting either the serial or the parallel clocks. Timing for each of the halves must be appropriate for the chosen outputs. For example, to operate the split serials using outputs A and B; S1a, S2ab, S3a and SWa would be clocked according to OUTa serial timing while S1b, S2ab, S3b, and SWb would be clocked according to OUTb serial timing. The parallels would be operated as for full-frame using either OUTa or OUTb parallel timing. To operate with a parallel split, the parallels would be operated in the quad split mode, while the serials would be clocked in the full-frame mode.

Timing diagrams for each output are shown in Figure 4. During a parallel or serial shift, the signal charge is transferred one pixel at a time. A full-frame readout consists of at least 2049 parallel shifts and serial readout sequences. Split parallel read out consists of 1025 shifts. Figure 5 shows the typical timing for a full frame readout. A serial readout sequence consists of at least 2088 serial shifts for the full-frame mode (20 for each serial extended region plus 2048 pixels of data from the imaging array) and 1044 (1024+20) shifts for split serial modes. The serials are static when the parallels are shifting and vice-versa. During integration, the serial clocks are normally kept running continuously to flush the serial registers and to stabilize the bias levels in the off-chip signal chain.

The timing diagram (Figure 4) is for integration under phases 1 and 2. For MPP operation, this timing is a requirement (as it is with all SITe MPP devices). For non-MPP operation this timing is also a desirable option, since the number of rows will remain the same as for MPP operation. For the users reference, typical timing for the clamp and sample signal of an external charge detection circuit are included in the output timing diagrams.

Multi-Phase Pinned (MPP) Operation

The multi-phase pinned (MPP) technology used on the SI-424A allows the device to be operated totally inverted during integration and line readout. The main advantage of this mode of operation is that it results in much lower dark current than with conventional CCD operation. Other advantages of MPP operation are the reduction of the surface residual image defect and a greater tolerance for ionizing radiation environments.

To operate the CCD in the MPP mode, the array clocks are biased sufficiently negative to invert the n-buried channel and "pin" the surface potential beneath each phase to the substrate potential. This allows holes from the p+ channel stop to populate the surface states at the silicon/silicon dioxide interface, minimizing surface dark current generation.

To enable all three phases of the array to be inverted and still retain well capacity, MPP devices have an extra implant under the phase 3 gates. During integration, this creates a potential barrier between each pixel allowing signal charge to accumulate under phases 1 and 2 at each pixel site. A consequence of this mode of operation is that the total well capacity is about 50 percent of that of a standard CCD if all the parallel clocks are operated at the same voltages. A larger well capacity can be obtained if phase 3 parallel clock high rail is operated about 3 volts higher than the phase 1 and phase 2 high rails.

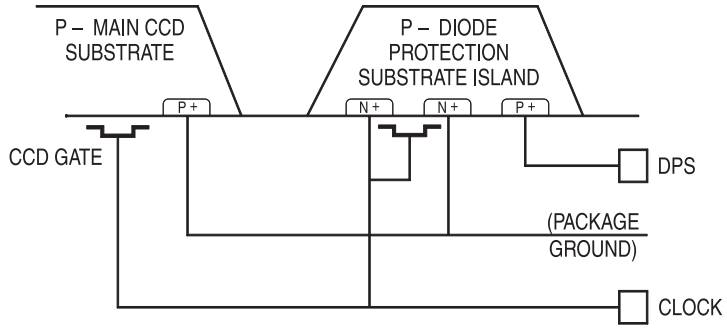
CCD ESD Gate Protection

Each ESD-sensitive gate on the SI-424A (back-illuminated) CCD contains a diode protection circuit to decrease the sensitivity of the device to ESD damage (see figure 2). The circuit consists of a physically isolated metal gate transistor. Its substrate (DPS) may be biased to approximately 1 volt below the lowest voltage applied to the CCD gates, or may be self biased by leaving DSP floating. For this structure to function properly, the substrate of the transistor must be electrically isolated from the main CCD substrate.

The isolation is accomplished during the thinning process on back-illuminated CCDs. This protection circuit is not included on front-illuminated devices.

When a voltage less than VDPS is applied to the gate terminal, the protection circuit will forward bias the PN junction and conduct current from the gate connection to the DPS connection. When a positive voltage greater than the breakdown of the transistor is applied to the gate terminal (typically 30V), the breakdown action will conduct current from the gate to the package ground connection. This effectively places a moderate resistance path to the substrate for large gate voltage excursions, aiding in ESD protection.

FIGURE 2 *Gate Protection Structure For Each Gate*



DEVICE SPECIFICATIONS

Measured at -45 deg. C, unless otherwise indicated, 45 kpixels/sec and standard voltages using a dual slope CDS circuit (8 µs integration time)

			Minimum	*Typical*	*Maximum*
Format				2048 x 2048 pixels	
Pixel Size				24 µm x 24 µm	
Imaging Area				49 mm x 49 mm	
Dark current (MPP), 20° C equivalent				50 pa/cm^2	100 pa/cm^2
NON-MPP (non inverted)				250 pa/cm^2	500 pa/cm^2
Readout noise	Front			5 electrons	10 electrons
	Back			7 electrons	10 electrons
Full Well signal			150,000 electrons	200,000 electrons	
Dynamic Range (relative to readout noise)			15,000:1	28,000 - 40,000:1	
Output gain			1.0 µV/ electron	1.3 µV/ electron	
CTE per pixel			0.99998	0.99999	
Output Amplifier Power Dissipation (each)				7 mW	
Clockline Capacitance[1]	parallel			230,000 pF	
	serial			600 pF	
Clockline Resistance[2]	front illuminated	phase 1		75 ohms	
		phase 2		55 ohms	
		phase 3		45 ohms	
	back illuminated	phase 1		185 ohms	
		phase 2		400 ohms	
		phase 3		460 ohms	
Clock Rise and Fall Times		Reset		0.2 µsec	
		Serial		0.2 µsec	
		Parallel		5.0 µsec	
Minimum Clock Overlap		Parallels		0.8 msec	
Quantum Efficiency				see Figure 7	

1 These are estimated values per phase for the entire array, and include phase to phase and phase to substrate capacitances.
2 These values are obtained with Pxa and Pxc connected together and with Pxb/Pxd connected together. Resistance is measured from Pxa to Pxb. It includes metal buss resistance and poly gate resistance in a series-parallel combination.

TABLE 1 *Device specifications, SI-424A*

DC OPERATING CONDITIONS

Terminal	*Item*	*Min.*	*Standard*	*Max.*	*Unit*
VDDx	Output Drain Supply	20	24.8	25	V
RDx	Reset Drain	12	13.4	16	V
LGx	Last Gate	-5	-3.5	5	V
SUB,PKG	Sub & Package Connection	-10	0	10	V
GNDx	MOSFET Ground Reference	-10	0	10	V
OUTx	MOSFET Output (Load)	5	15	50	kohms
DPS*	Diode Protection Substrate	11	-9	**	V

* For back-illuminated devices only. Terminal is not connected on front-illuminated devices.
** Most negative gate voltage.

GATE TO SUBSTRATE VOLTAGES

Terminal	*Item*		*Min.*	*Standard*	*Max.*	*P to P Max.*	*Unit*
RGx	Reset Gate	Low Rail	-5	0	5	20	V
		High Rail	7	12	18		V
S#x	Serial Gate	Low Rail	-10	-5	0	20	V
		High Rail	5	7	15		V
Wx	Summing Well	Low Rail	-10	-4	0	20	V
		High Rail	0	4.5	15		V
P#x	Parallel Gate	Low Rail	-10	-8.5	0	20	V
		High Rail	0	4.5	15		V
P3		High Rail	0	7.5	15		V
TGx	Transfer Gate	Low Rail	-10	-8.5	0	20	V
		High Rail	0	7	15		V

TABLE 2 *DC operating conditions and clock voltages, SI-424A*

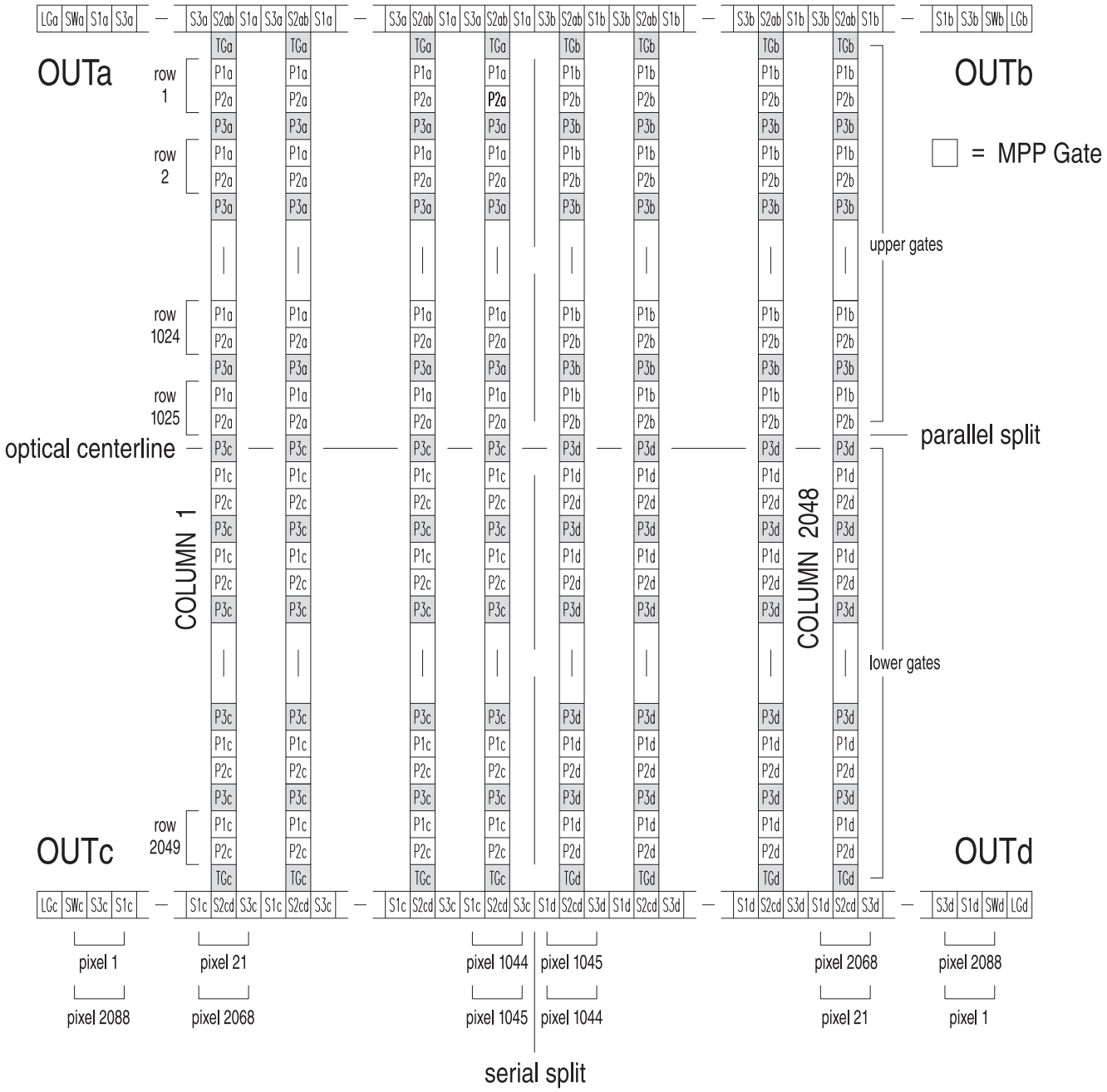


FIGURE 3 *SI-424A functional diagram*

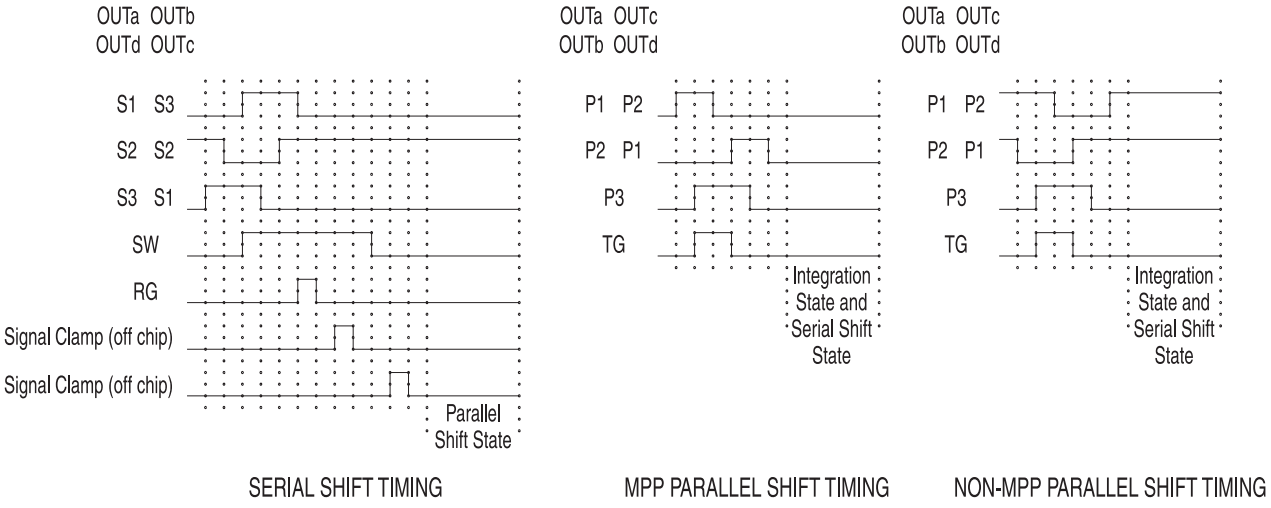


FIGURE 4 *Serial and parallel timing for all outputs*

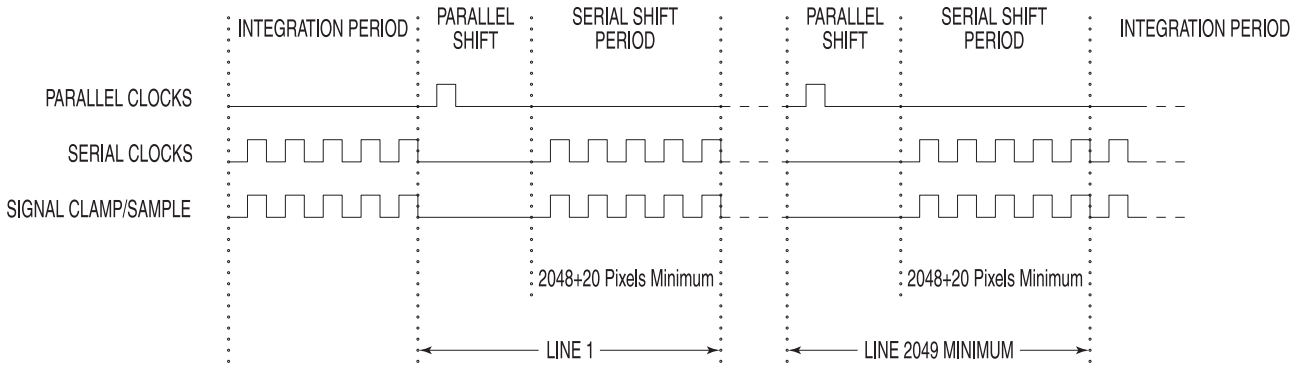


FIGURE 5 *Typical full-frame readout*

SI-424A PIN DEFINITION							
PIN # (Back)	***Function***	***Registers***	***Symbol***	***PIN # (Back)***	***Function***	***Registers***	***Symbol***
1	Substrate and Package Ground		SUB	41	Substrate and Package Ground		PKG
2	Output transistor source, c output	c register	OUTc	42	Output transistor source, b output	b register	OUTb
3	Reserved	*	Res	43	Reserved	*	Res
4	Reset Drain Supply, c output	c register	RDc	44	Reset transistor drain, b output	b register	RDb
5	Reset Gate, c output	c register	RGc	45	Reset transistor gate, b output	b register	RGb
6	Last gate, c output	c register	LGc	46	Last gate, b output	b register	LGb
7(8)	Serial phase 3, c register	c register	S3c	47(48)	Serial phase 3, b register	b register	S3b
8(7)	Serial phase 1, c register	c register	S1c	48(47)	Serial phase 1, b register	b register	S1b
9	Serial phase 2, common cd register	cd register	S2cd	49	Serial phase 2, common ab register	ab register	S2ab
10	Serial phase 2, common cd register	cd register	S2cd	50	Serial phase 2, common ab register	ab register	S2ab
11(12)	Serial phase 1, d register	d register	S1d	51(52)	Serial phase 1, a register	a register	S1a
12(11)	Serial phase 3, d register	cd register	S3d	52(51)	Serial phase 3, a register	a register	S3a
13	Last gate, d output	d register	LGd	53	Last gate, a output	a register	LGa
14	Reset transistor gate, d output	d register	RGd	54	Reset transistor gate, a output	a register	RGa
15	Reset transistor drain, d output	d register	RDd	55	Reset transistor drain, a output	a register	RDa
16	Reserved	*	Res	56	Substrate and Package Ground		PKG
17	Output transistor source, d output	d register	OUTd	57	Output transistor source, a output	a register	OUTa
18	Substrate and Package Ground		PKG	58	Diode Protection substrate		DPS
19	Output transistor drain, d output	d register	VDDd	59	Output transistor drain, a output	a register	VDDa
20	Output Ground Reference	d register	GNDd	60	Output Ground Reference	a register	GNDa
21	Summing well, d output	d register	SWd	61	Summing well, a output	a register	SWa
22	Transfer gate, lower serial register	cd register	TGd	62	Transfer gate, upper serial register	ab register	TGa
23	Parallel phase 3	lower quadrants	P3d	63	Parallel phase 3	upper quadrants	P3a
24	Parallel phase 1	lower quadrants	P1d	64	Parallel phase 1	upper quadrants	P1a
25	Reserved	*	Res	65	Reserved	*	Res
26	Reserved	*	Res	66	Reserved	*	Res
27	Parallel phase 2	lower quadrants	P2d	67	Parallel phase 2	upper quadrants	P2a
28	Reserved	*	Res	68	Reserved	*	Res
29	Temp. Sense Diode and Resistor		TD1/TR1	69	Temp. Sense Resistor		TR3
30	Temp. Sense Resistor		TR3	70	Temp. Sense Diode and Resistor		TD2/TR4
31	Reserved	*	Res	71	Reserved		Res
32	Parallel phase 2	upper quadrants	P2b	72	Parallel phase 2	lower quadrants	P2c
33	Reserved	*	Res	73	Reserved	*	Res
34	Reserved	*	Res	74	Reserved	*	Res
35	Parallel phase 1	upper quadrants	P1b	75	Parallel phase 1	lower quadrants	P1c
36	Parallel phase 3	upper quadrants	P3b	76	Parallel phase 3	lower quadrants	P3c
37	Transfer gate, upper serial register	ab register	TGb	77	Transfer gate, lower serial register	cd register	TGc
38	Summing well, b output	b register	SWb	78	Summing well, c output	c register	SWc
39	Output Ground Reference	b register	GNDb	79	Output Ground Reference	c register	GNDc
40	Output transistor drain, b output	b register	VDDb	80	Output transistor drain, c output	c register	VDDc

NOTES: The signals applied to pins 7, 8, 11, 12, 47, 48, 51, and 52 are different for front and back-illuminated parts. The amplifier ground references (GNDx) are local substrate connections, intended for signal chain reference. They should not be biased differently than the other substrate or package connections.

* This is a package connection on the current version; future versions may omit this connection.

TABLE 3 *SI-424A pin definitions*

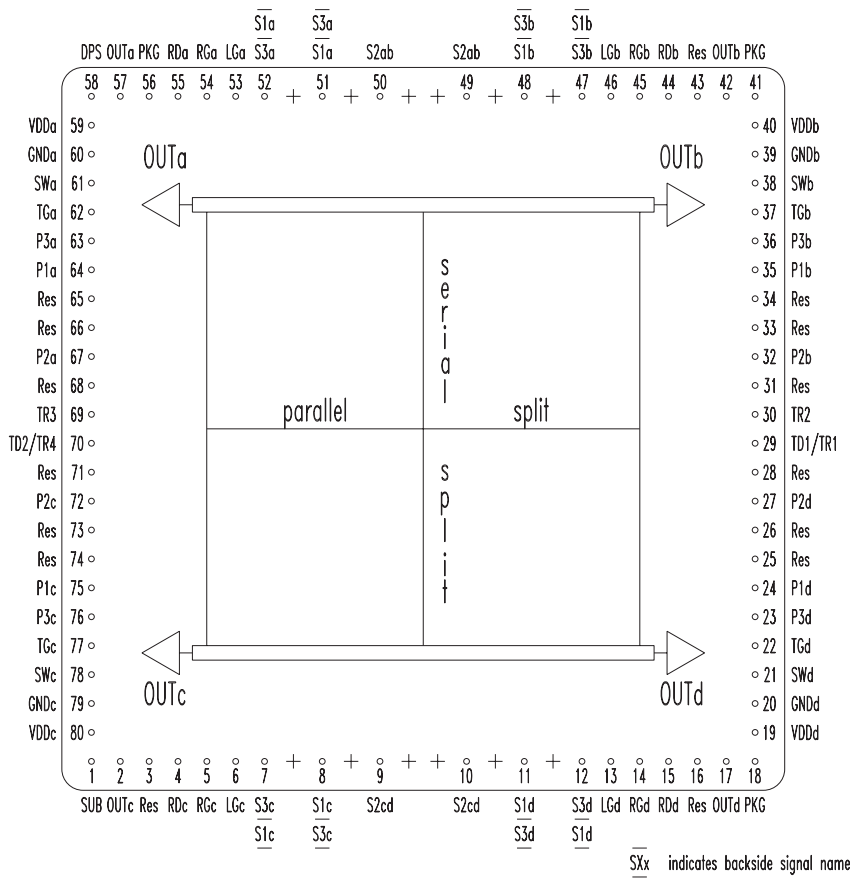


FIGURE 6 *SI-424A pin labels*

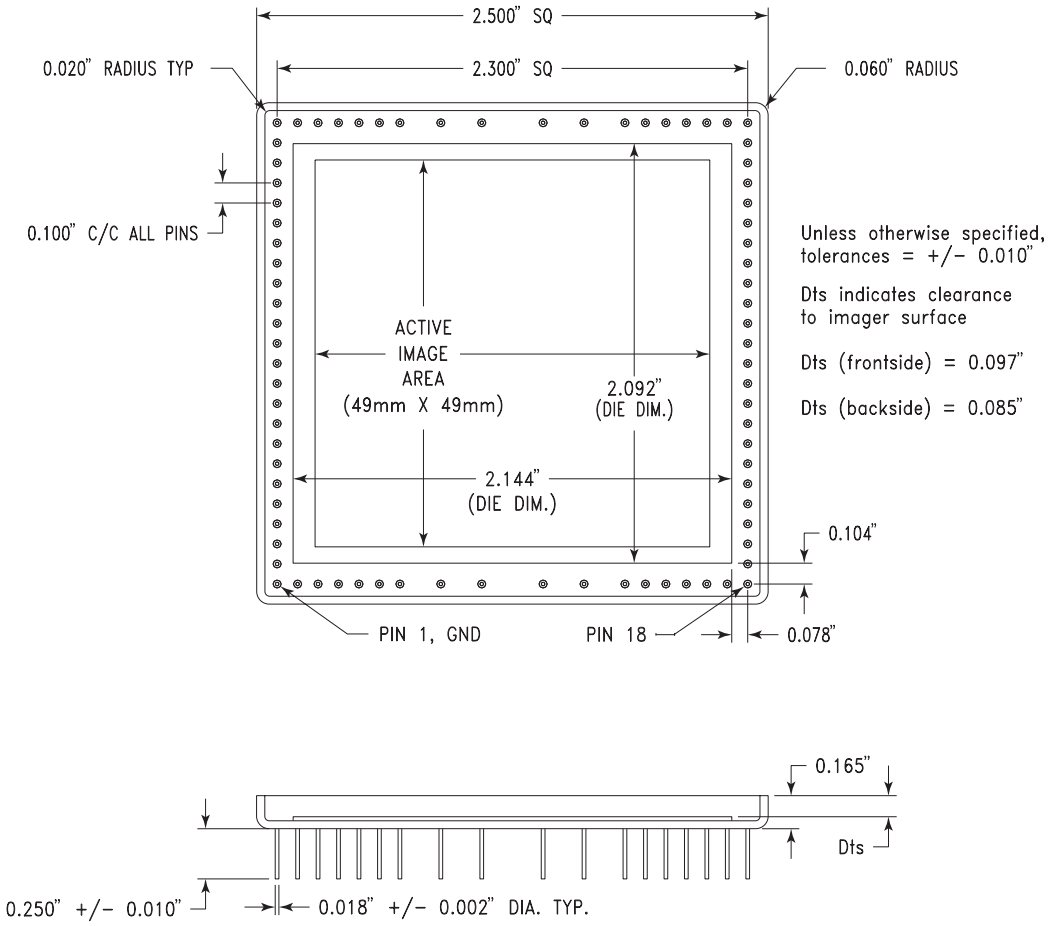


FIGURE 7 *SI-424A package configuration*

NOTE: **Please contact SITe for any current revisions to the above drawings and dimensions.**

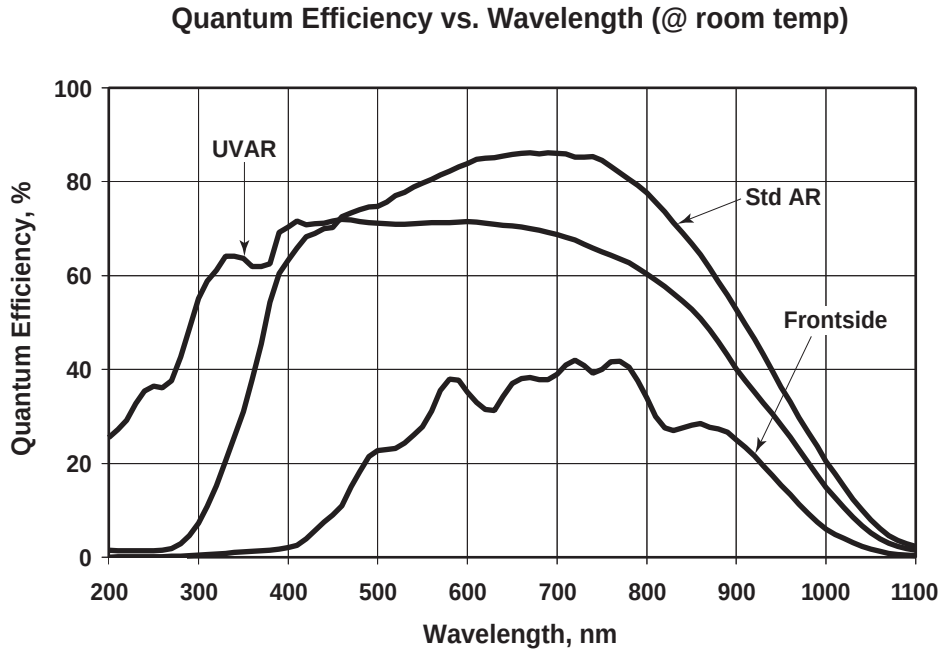


FIGURE 8 *Typical QE curves*

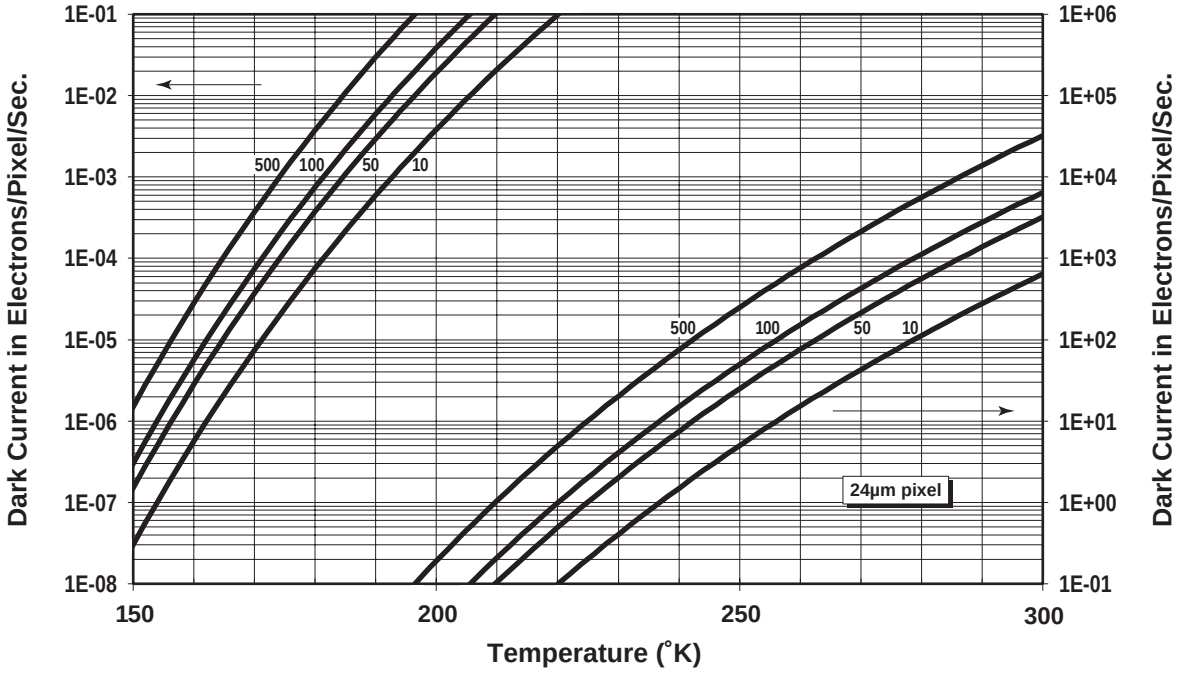


FIGURE 9 *Effect of temperature on dark current. Parameter is pAmp/cm^2 at 293K*