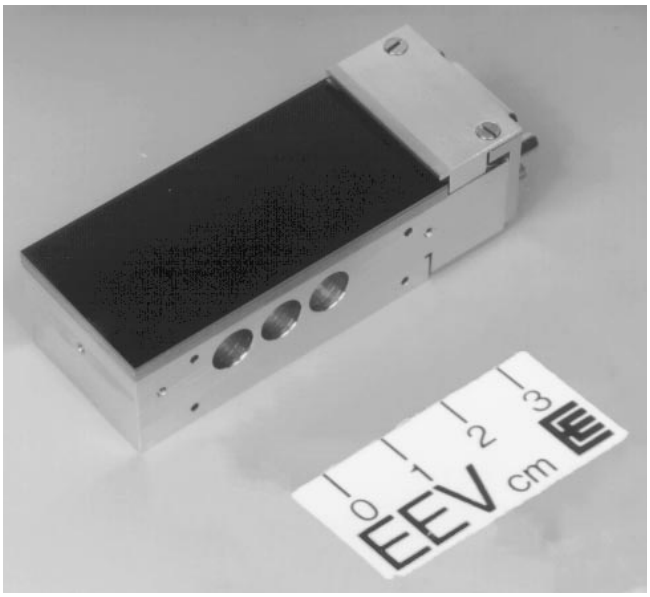
CCD42-80 Back Illuminated High Performance CCD Sensor

FEATURES

- 2048 by 4096 Pixel Format
- 13.5 µm Square Pixels
- Image Area 27.6 x 55.3 mm
- Wide Dynamic Range
- Symmetrical Anti-static Gate Protection
- Back Illuminated Format for Enhanced Quantum Efficiency
- 3-side Buttable Close Butting Package
- Gated Anti-blooming Readout Register
- Low Noise Variable Gain Output Amplifier
- Flatness better than 15 µm peak to valley



APPLICATIONS

- Astronomy
- Scientific Imaging

INTRODUCTION

This version of the CCD42 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with an extremely low noise amplifier, makes the device well suited to the most demanding applications, such as astronomy. To further improve sensitivity, the CCD is manufactured without anti-blooming structures.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional scientific CCDs at pixel rates as high as 1 MHz.

The readout register has a gate controlled dump-drain to allow fast dumping of unwanted data. The register is designed to accommodate four image pixels of charge and a summing well is provided capable of holding six image pixels. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics and is designed to be used cryogenically. The design of the package will ensure that the device flatness is maintained at the working temperature.

TYPICAL PERFORMANCE

Pixel readout frequency	20 - 1000	kHz
Output amplifier sensitivity	4.5	µV/e^-
Peak signal	150	ke^-/pixel
Spectral range	200 - 1060	nm
Readout noise (at 188 K, 20 kHz)	3	e^- rms
QE at 500 nm	90	%
Peak output voltage	675	mV

GENERAL DATA

Format

Image area	27.6 x 55.3	mm
Active pixels (H)	2048	
(V)	4096 + 4	
Pixel size	13.5 x 13.5 µm	

Package

Package size	77.25 x 28.168	mm
Number of pins	36	
Window material	N/A	
Inactive edge spacing:		
sides	280	µm
top	150	µm

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	100k	150k	-	e^-/pixel
Peak output voltage (unbinned)		675		mV
Dark signal at 153 K (see note 2)		<0.1	4	e^-/pixel/hour
Charge transfer efficiency (see note 3):				
parallel	99.999	99.9999		%
serial	99.999	99.9993		%
Output amplifier sensitivity	3.0	4.5	6.0	μV/e^-
Readout noise at 188 K (see note 4)		3	4	rms e^-/pixel
Readout frequency (see note 5)	-	20	1000	kHz
Output node capacity				
OG2 high	-	1000k	-	electrons
OG2 low	-	200k	-	electrons

Spectral Response

Wavelength (nm)	Spectral Response (QE) Typical	Spectral Response (QE) Min	Response Non-uniformity, max (1σ)	
350	50	40	5	%
400	80	70	3	%
500	90	80	3	%
650	80	75	3	%
900	30	25	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

	Min	Typical	Max	
IØ/IØ interphase	-	TBD	-	nF
RØ/RØ interphase	-	TBD	-	pF
IØ/SS	-	TBD	-	nF
RØ/SS	-	TBD	-	pF
Output impedance	-	TBD	-	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. Dark signal is typically measured at 188 K and $V_{ss} = +9$ V. The dark signal at other temperatures may be estimated from:

   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

   where Q_{d0} is the dark current at 293 K.
3. Measurements made using charge generated by X-ray photons of known energy.
4. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period with OG2 = OG1 + 1 V.
5. Readout above 1000 kHz can be achieved but performance to the parameters given cannot be guaranteed.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 188 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a responsivity of less than 80% of the local mean signal.

White spots Are counted when they have a generation rate equivalent to 100 electrons per pixel per hour at 153 K (typically measured at 188 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

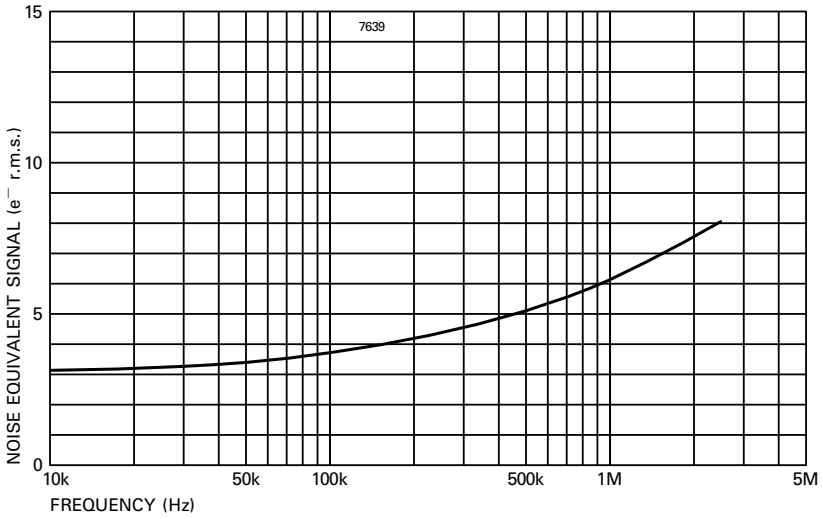
$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

Column defects A column which contains at least 100 white or black defects.

GRADE	0	1	2
Column defects	2	6	12
Black spots	500	750	1000
Traps >200 e^-	15	30	50
White spots	250	400	600

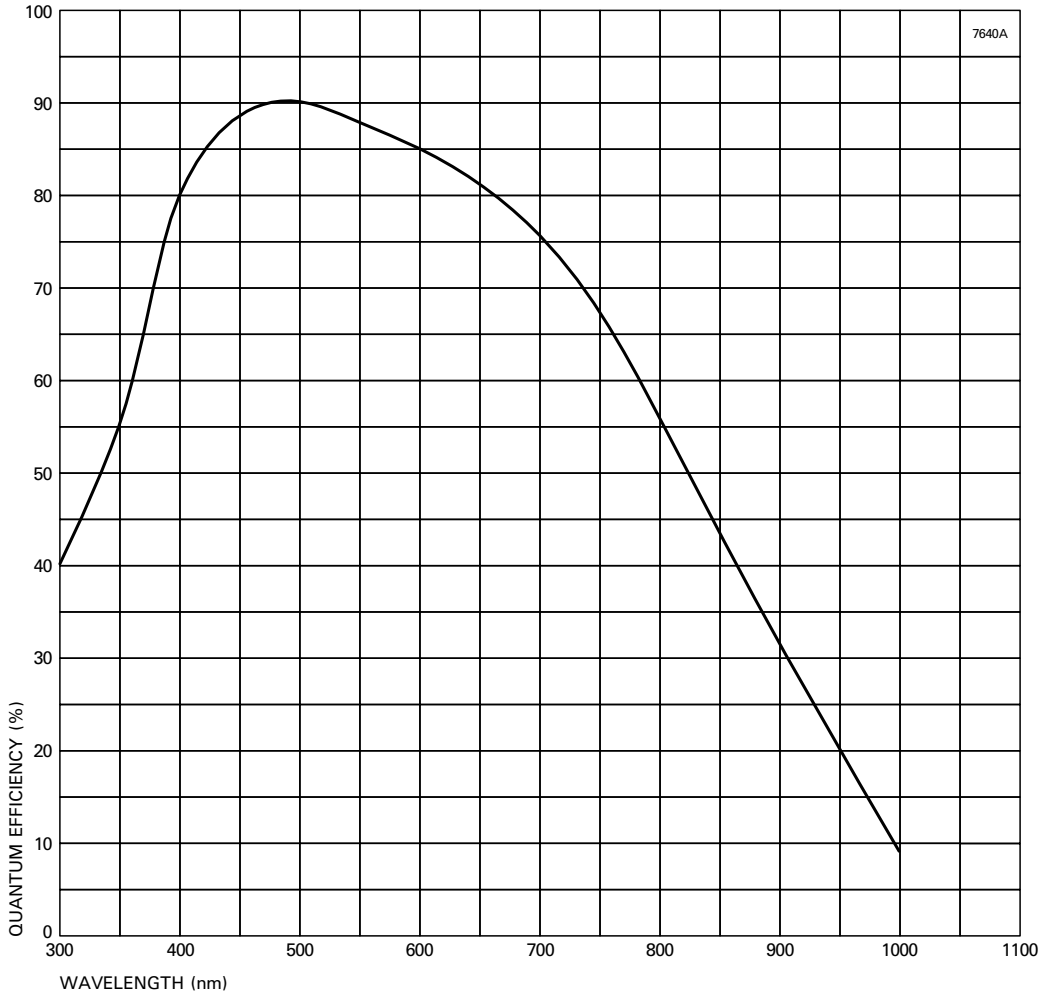
TYPICAL OUTPUT CIRCUIT NOISE

(Measured using clamp and sample, temperature range 140 - 230 K)

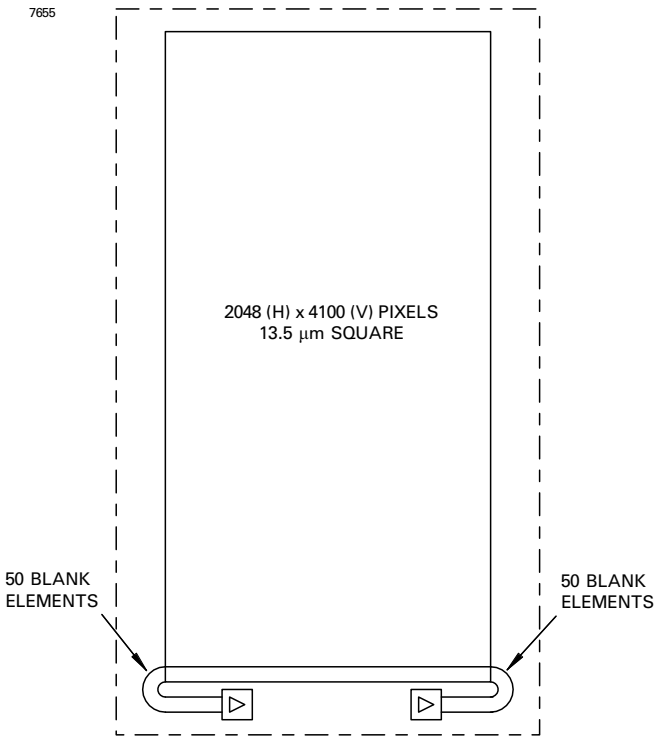


TYPICAL SPECTRAL RESPONSE

(At −90 °C, measured with astronomy broadband AR coating)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

21-pin Micro D-connector

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	SW(L)	Summing well (left)		CLOCK AS RØ3		±20 V
2	DG	Dump gate (see note 6)	-	0	-	±20 V
3	ØR(L)	Reset gate (left)	9	12	15	±20 V
4	RØ2(L)	Register clock phase 2 (left)	9	11	15	±20 V
5	RØ1(L)	Register clock phase 1 (left)	9	11	15	±20 V
6	RØ3	Register clock phase 3	9	11	15	±20 V
7	RØ1(R)	Register clock phase 1 (right)	9	11	15	±20 V
8	RØ2(R)	Register clock phase 2 (right)	9	11	15	±20 V
9	ØR(R)	Reset gate (right)	9	12	15	±20 V
10	DG	Dump gate (see note 6)	-	0	-	±20 V
11	SW(R)	Summing well (right)		CLOCK AS RØ3		±20 V
12	OG1(L)	Output gate 1 (left)	1	2	3	±20 V
13	SS	Substrate	0	9	10	-
14	IØ2	Image area clock, phase 2	8	10	14	±20 V
15	IØ1	Image area clock, phase 1	8	10	14	±20 V
16	IØ3	Image area clock, phase 3	8	10	14	±20 V
17	-	No connection	-	-	-	-
18	-	No connection	-	-	-	-
19	-	No connection	-	-	-	-
20	SS	Substrate	0	9	10	-
21	OG1(R)	Output gate 1 (right)	1	2	3	±20 V

NOTE

6. Non-charge dumping level shown. For operation in charge dumping mode DG should be pulsed to 12±2 V.

15-pin micro D-connector

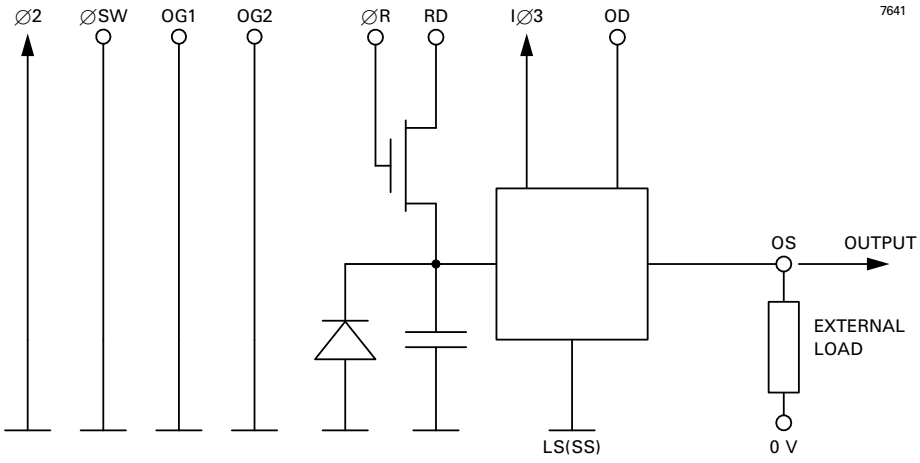
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6)			MAXIMUM RATINGS with respect to $V_{S\ S}$
			Min	Typical	Max	
1	DD	Dump drain	22	24	26	−0.3 to 30 V
2	RD (L)	Reset drain (left)	15	17	19	−0.3 to 30 V
3	OG2(L)	Output gate 2 (left)		see note 7		±20 V
4	-	No connection	-	-	-	-
5	-	No connection	-	-	-	-
6	OG2(R)	Output gate 2 (right)		see note 7		±20 V
7	RD(R)	Reset drain (right)	15	17	19	−0.3 to 25 V
8	DD	Dump drain	22	24	26	−0.3 to 30 V
9	OD(L)	Output drain (left)	27	29	31	−0.3 to 35 V
10	OS(L)	Output transistor source (left)		see note 8		−0.3 to 25 V
11	SS	Substrate	0	9	10	-
12	SS	Substrate	0	9	10	-
13	SS	Substrate	0	9	10	-
14	OS(R)	Output transistor source (right)		see note 8		−0.3 to 25 V
15	OD(R)	Output drain (right)	27	29	31	−0.3 to 35 V

If all voltages are set to the typical values operation at, or close to, specification should be obtained. Some adjustment within the minimum - maximum range specified may be required to optimise performance.
Maximum voltage between pairs of pins: OS to OD ±15 V.
Maximum current through any source or drain pin: 10 mA.

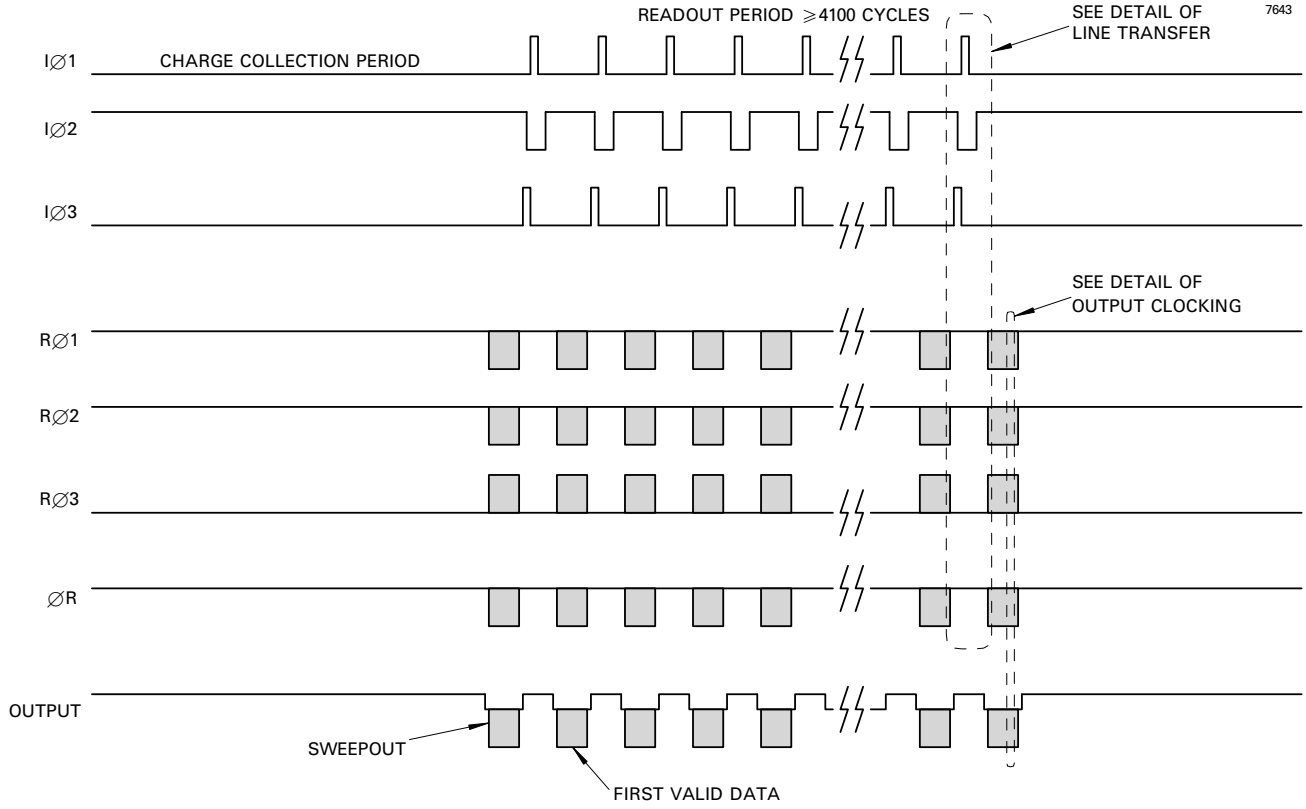
NOTES

7. OG2 = OG1 + 1 V for operation of the output mode in high responsivity, low noise mode. For operation at low responsivity high signal OG2 should be set to +20 V
8. Not critical; can be a 3 to 5 mA constant current source, or 5 to 10 kΩ resistor.
9. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
10. With the R∅ connections shown this device will operate through both outputs simultaneously. In order to operate from the left hand output only R∅1(R) and R∅2(R) should be reversed.

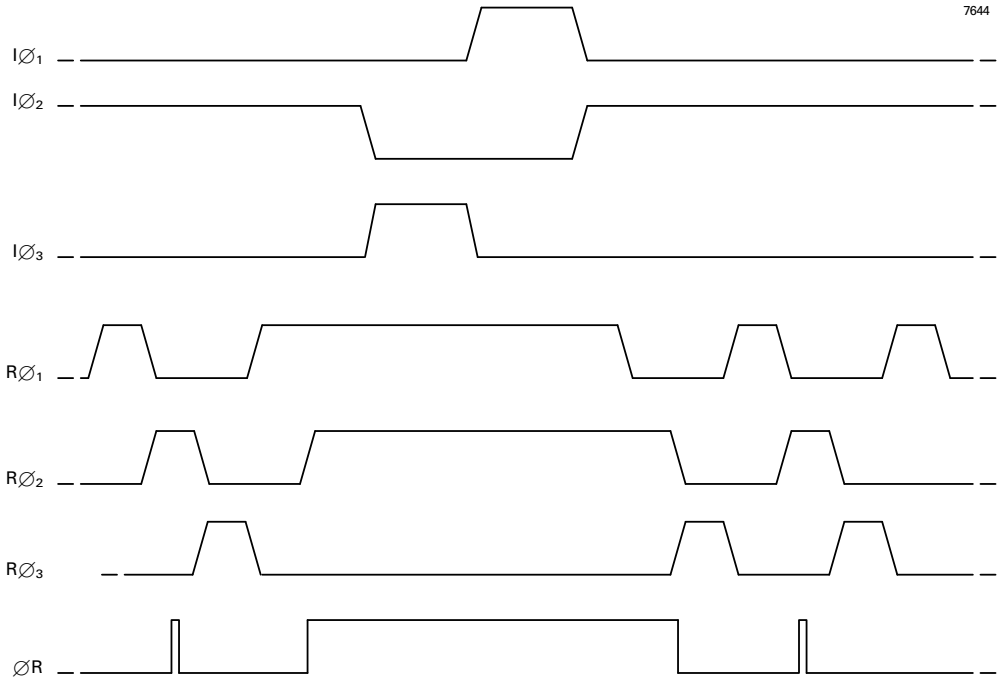
OUTPUT CIRCUIT



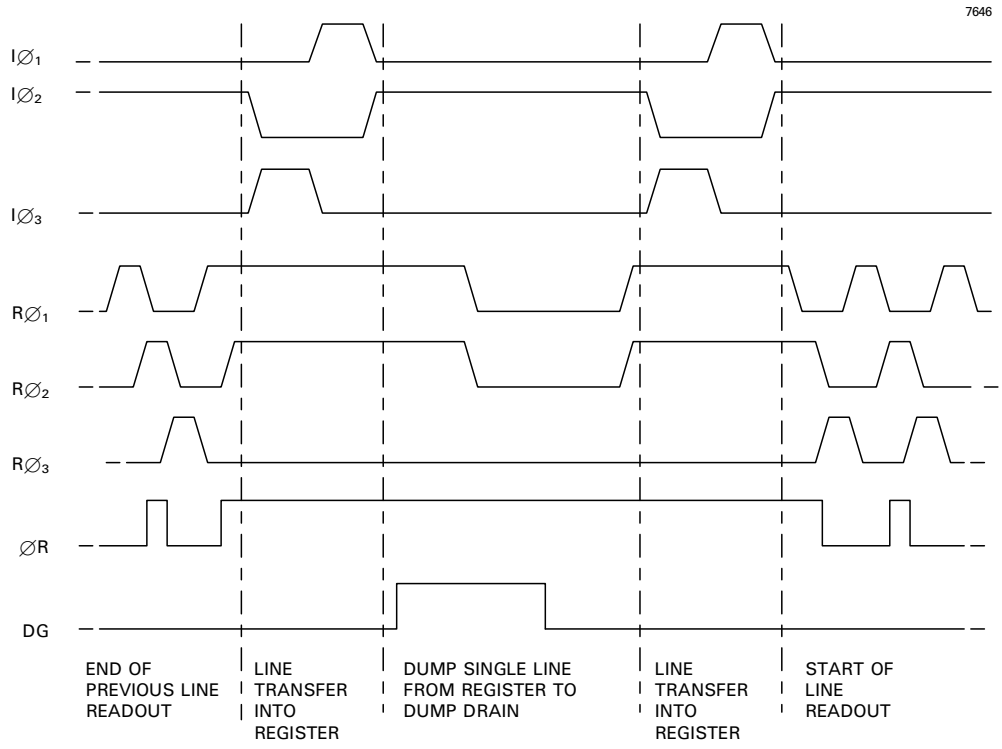
FRAME READOUT TIMING DIAGRAM



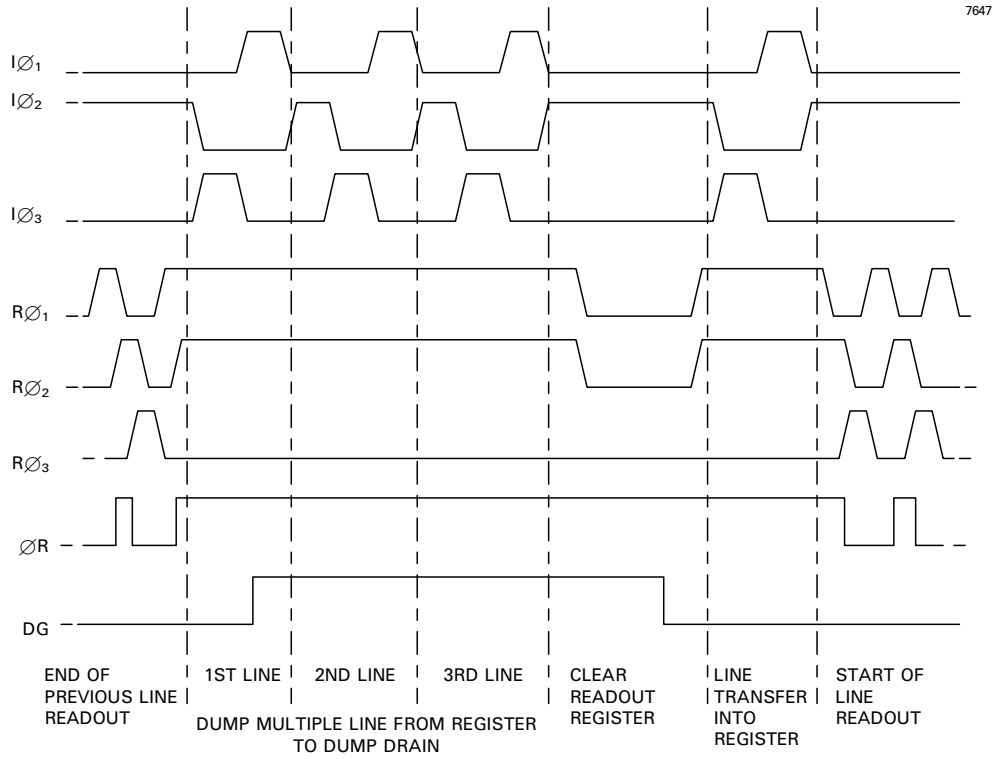
DETAIL OF LINE TRANSFER



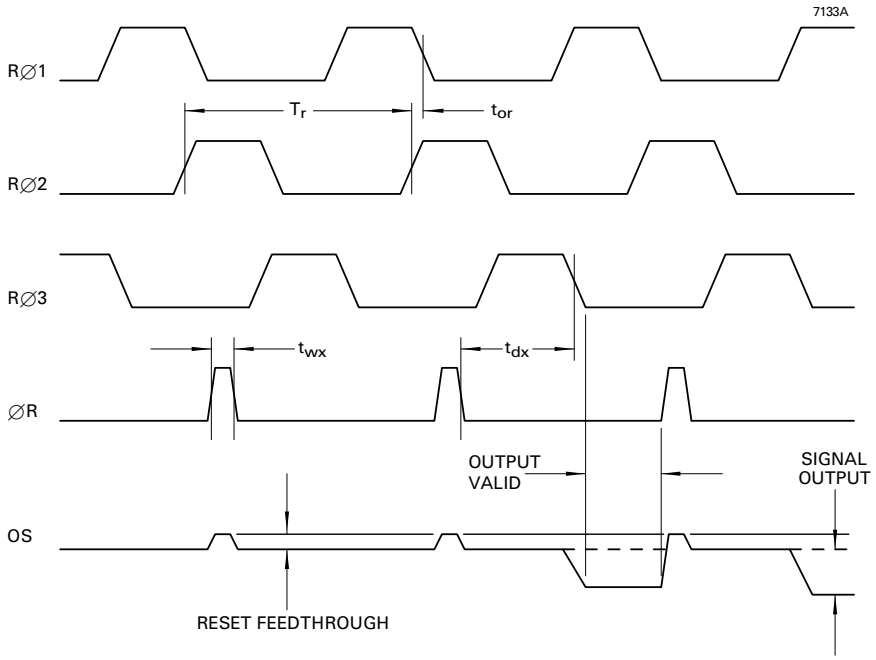
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



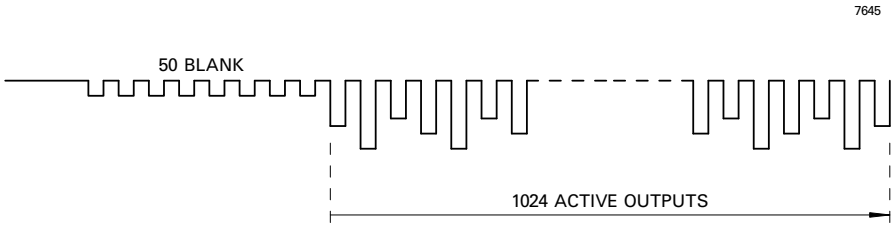
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



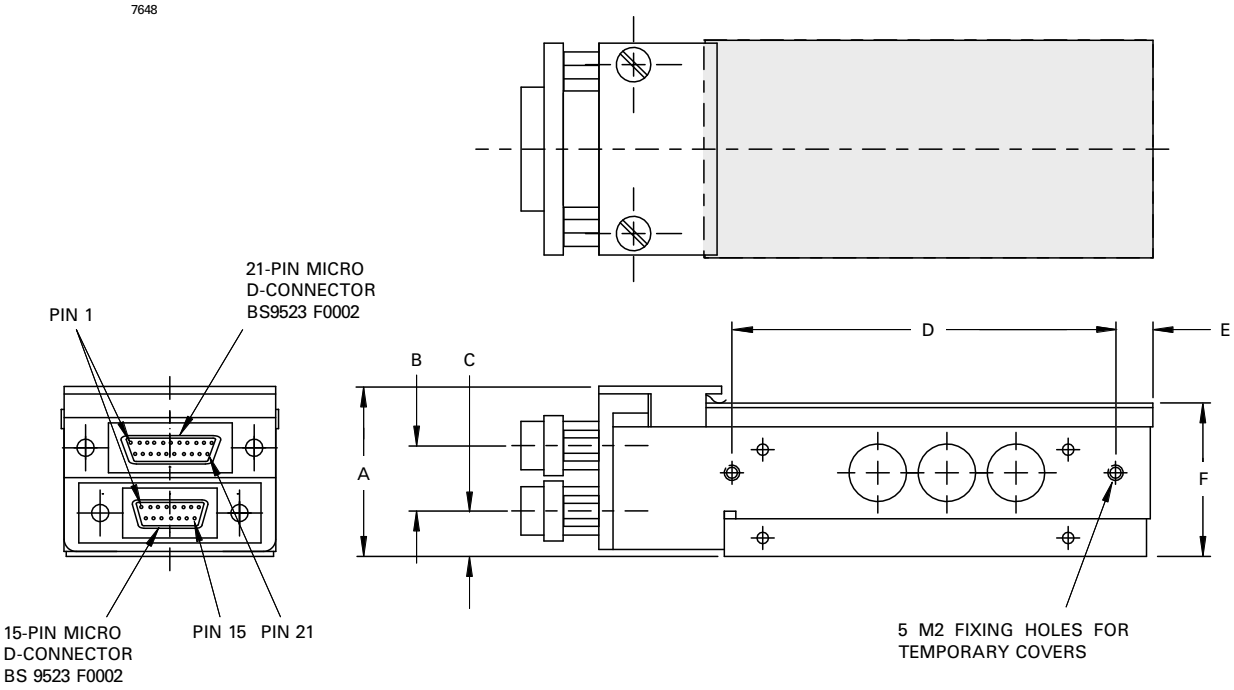
CLOCK TIMING REQUIREMENTS

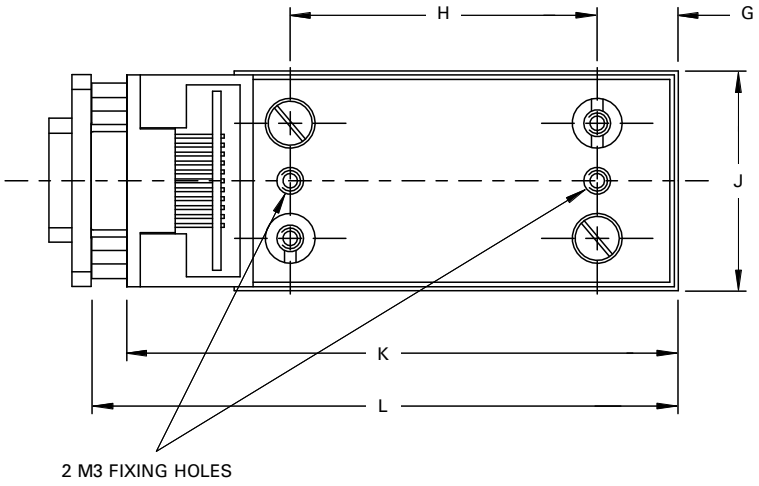
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	50	100	see note 11	µs
t_{wi}	Image clock pulse width	25	50	see note 11	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	5	10	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	10	20	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	10	20	see note 11	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 11	µs
T_r	Output register clock cycle period	1	see note 12	see note 11	µs
t_{rr}	Clock pulse rise time (10 to 90%)	100	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	50	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	50	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	50	$0.5T_r$	$0.8T_r$	ns

NOTES

11. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
12. As set by the readout period.

OUTLINE
(All dimensions without limits are nominal)





Ref	Millimetres
A	22.50
B	8.50
C	6.00
D	50.00
E	4.83
F	20.00 ± 0.015
G	10.83
H	40.00
J	28.168 ± 0.010
K	72.60
L	77.25

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 21 on the 21-pin micro D-connector and pins 3 and 6 on the 15-pin micro D-connector) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to greater than 10^4 rads. This corresponds to:

10^{13} of 15 MeV neutrons/cm^2
2×10^{13} of 1 MeV gamma/cm^2
4×10^{11} of ionising particles/cm^2

Certain characterisation data are held at EEV. Users planning to use CCDs in a high radiation environment are advised to contact EEV.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	153	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . 5 K/min