TEK 4 Voltages

This shows what voltages you can expect at the SDSU front panel
and at the cryostat connector

CCD Pin	flanged 20-41	Function	SDSU controller mixed D connector	Voltage		
				Bias	Clock Hi	Clock Lo
49,23	H	V2u	8		4	-8
51,21	g	V2l	8		4	-8
50,22	P	V3	9		8	-8
48,24	K	V1u	17		4	-8
52,20	k	V1l	17		4	-8
47,25	M	TGu	3		5	-5
53,19	i	TGl	16	-5		
38	G	S1a	5		10	-2
34	R	S1b	5		10	-2
6	j	S1c	14	10		
10	b	S1d	14	10		
37	J	S2a	6		10	-2
35	N	S2b	6		10	-2
7	h	S2c	14	10		
9	d	S2d	14	10		
36	L	S3ab	7		10	-2
8	f	S3cd	14	10		
46	F	SWa	1		8	-1
26	S	SWb	1		8	-1
54	n	SWc	14	10		
18	e	SWd	14	10		
40	E	PhiRa	4		10	0
32	T	PhiRb	4		10	0
4	p	PhiRc	14	10		
12	Z	PhiRd	14	10		
42,30,14,2	Y	SUB	12	0		
55,45,27,17	D	GND	12	0		
39,33,11,5	m	LG	2	0.5		
41	C	RDa	15	13		
31	V	RDb	15	13		
3	r	RDc	15	13		
13	X	RDd	15	13		
44	B	ODa	11	23		
43	A	OSa	**A3**			
28	U	ODb	11	23		
29	W	OSb	**A2**			
56	q	ODc	15	13		
1	s	OSc	15	13		
16	c	ODd	15	13		
15	a	OSd	15	13		