ING Technical Note 131

Conversion of ING Cameras to SDSU Generation 3
Controllers

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1. Need for the upgrade

There are now approximately 25 SDSU systems at ING, with more planned. Their reliability and the availability of spares are of critical operational importance. We need to continue to buy spares in an ongoing fashion to maintain this reliability. There is now the option of Generation III controllers which offer improved performance and reliability at the same price as the Gen II alternative. With these new controllers available it makes no sense to continue buying older Gen II controllers with their obsolete components.

Two cameras have been converted to Gen III operation. They have been tested with both the ARC supplied 'Voodoo' program and uDAS. The conversion was fairly complex but having converted these two cameras, the conversion of the rest should be straightforward and rapid. This document describes the changes required in the conversion of a camera to Gen III.

2. Hardware Differences between Gen. II and III Controllers

The PCi interface card that sits in the SPARC/PC and the timing card in the controller itself are completely different. In Gen III the fibre link that connects these two elements runs at a speed of 12.5MPix/s, in Gen II it is only 2.5MPix/s. The Gen II fibre receiver/transmitters are obsolete. The processors on the timing boards are also completely different. Gen II uses a 50MHz DSP56002 (obsolete), Gen III a 100MHz DSP56303. The GenIII Timing board has a 25 way D connector that adds some extra features. The pins of this connector are described below:

Pin	Description
1	External clock in
2	Internal clock out
3	I/O PB11 of DSP
4	I/O PB10 of DSP
5	I/O PB13 of DSP
6	I/O PB12 of DSP
7	Serial interface
8	Serial interface

The digital IO pins leading directly to the processor could be useful for synchronizing the readout to external processes.

The newer processor in the Gen III timing board gives certain advantages, for a start it is twice as fast. It also has 4KWord of fast and 128Kwords of slow P: memory; plenty big enough even for the most ambitious applications. It has 2Kwords of fast X: and Y: memory where waveform and command tables are typically stored. By comparison the Gen III timing card has only 512 words of fast and 2Kwords of slow P: memory, 256 words of fast X: and Y: memory, 8Kwords of slow X: memory and 16K words of slow Y: memory. Gen II fast memory is not big enough and the GLAS WFS applications use every last word of it. Note that Gen II had more total X: and Y: memory than Gen III. The only time large amounts of this memory were ever used was in mode1 of the NAOMI L3 WFS. Here the 7040 pixel image was internally buffered and reformatted prior to transmission. This could be done on a Gen III controller but it would require using the slow P: memory as an image buffer.

The utility, clock and video processor cards will all work unmodified with either Gen II or Gen III. However, the utility card EEPROMS will need to be re-blown to include new code that communicates with the Gen III timing card.

Transferring to Gen III will give a slight increase in readout speed due to the fact that the software loops that read the columns and rows will execute faster in the higher speed processor. However, the major time elements in the readout of a CCD are the clock delays and these will be the same on both controllers. The new controller could give a big speed gain in multi-channel readouts where the fibre link is the bottle-kneck. The INGRID and LIRIS code could probably be rewritten to exploit this.

3. Software Differences between Gen. II and III Controllers

The driver for the Gen II PCi card also works with the Gen III card. Almost all the rest of the controller software needs to be rewritten, that is:

> Utility EEPROM (done)
> Utility application lod file (done)
> Timing EEPROM (done)
> Timing application lod file (conversion ongoing)

4. Cost of upgrading to Gen III

The upgrade requires, for each existing controller, the purchase of the two boards from Astronomical Research Camera (ARC) totaling $5500. These boards are the ARC-22 Timing board and the ARC-64 PCi board.

5. Programming Details associated with the upgrade.

5.1. uDAS noticeboards
UltraDas expects to find camera status information in 3 noticeboard areas of the timing board RAM as well as 3 additional areas of the utility board. These areas are called the P, X and Y noticeboard on account of the memory areas in which they are located. The location of the Timing P: noticeboard is invariable and must occupy locations P:$01FE and P:$01FF ; the top two locations in the fast ram of the SDSUII timing board. These two locations contain pointers to the X and Y noticeboard areas. Unfortunately the P: noticeboard location falls right in the middle of the ARC supplied timing boot code. This required some relocation of code and the addition of a jump statement to carry the program flow over the P: noticeboard area.

5.2. Timing delays
The waveform tables that define the CCD clock waveforms occupy the lower part of Y: memory on the timing board. A typical fragment from one of these tables is shown below :

       DC   CLK2+S_DELAY+PhRL+H1L+H2L+H3H
       DC   CLK2+S_DELAY+PhRH+H1L+H2L+H3H

The value of S_DELAY tells the clock board how long it must maintain the clocks at the defined state. It can have a value between 40ns and about 20μs. The delay is actually a 24 bit word. When modifying code to run on the Gen III timing board , the value of the delay word must be changed since the delay units on Gen III are twice as long as Gen II.

 The table below shows a few examples :

Required delay	Delay word Gen II	Delay word Gen III
0.5μs	$150000	$b0000
1 μs	$2e0000	$180000
1.5 μs	$470000	$250000
2.0 μs	$600000	$310000
5μs	$9f0000	$8f0000
10μs	$be0000	$9f0000
40 ns	$000000	$000000
80 ns	Not possible	$010000
100 ns	$010000	Not possible
120 ns	$020000	$020000
140 ns	$030000	Not possible
160 ns	$040000	$030000
180 ns	$050000	Not Possible
200 ns	$060000	$040000

Since no documentation is available for the new timing board, these values were arrived at empirically. As with Gen II it is bit 23 of the delay word that defines what the time units of the delay are , if the bit is set the delay units are 320ns, if clear they are 40ns. An overhead of 40ns must then be added to the calculated value. The minimum delay is still 40ns, despite the processor being twice as fast. This is a major disappointment since it was originally intended that the system should clock twice as fast. If this extra speed were available in future versions of the clock board it would make a huge difference to the readout speeds of ING cameras.

5.3. ADC Data transmission

The Timing board hardware offers a fast method of transferring data from ADCs to fibre transmitter. A PAL is included that transfers data directly without it having to pass through the processor. This is particularly useful when several channels of data are being generated. The PAL transfer can be activated by a write of the 'SXMIT' word to the clock board. The word is intercepted by the PAL situated on the timing board and used to force a delay in processing for the requested period. The value of this word is interpreted according to the following table. Notice that it is different for the two generations of timing board:

ADC channels to be transmitted	SXMIT value Gen II	SXMIT value Gen III
#0 only	$00F000	$00F000
#1 only	$00F021	$00F041
#2 only		$00F082
#3 only		$00F0C3
#0 and #1	$00F020	$00F040
#0,#1,#2 and #3	$00F060	$00F0C0

Again, no Gen III documentation is available on the exact values of SXMIT for other ADC channel combinations. The three values shown above were deduced from source code supplied by ARC.

5.4. Assembler locations

Copies of the DSP56303 assembler, linker, s-record and lod file generator programs were downloaded from the Motorola/Freescale Semiconductor web site and installed in the following locations:

assembler	/home/dspdev/SUNW56300/asm56300
linker	/home/dspdev/SUNW56300/dsplnk
lod file generator	/home/dspdev/SUNW56300/cldlod
s-record generator	/home/dspdev/SUNW56300/srec

The equivalent programs used to assemble Gen II timing and Utility code are located in:

Assembler	/home/dspdev/SUNW56000/asm56000
linker	/home/dspdev/SUNW56000/dsplnk
lod file generator	/home/dspdev/SUNW56000/cldlod
s-record generator	/home/dspdev/SUNW56000/srec

5.5. The CLOCK subroutine

This is a very useful subroutine supplied by ARC that takes the address of a waveform table as a parameter in the R0 register and then transmits that whole table sequentially to the clock board. In the Gen II version of this subroutine the first word of the table must be equal to the length of the table-2. In the Gen III version this first word must be equal to the length -1. The clock tables must be a minimum of three lines long.

5.6. Blowing EEPROMS

The new s-record files generated for the timing and utility boot EEPROMS can be downloaded directly into the S4 programmer and blown without any code relocation.
Since there are three utility EEPROMS there are 3 s-records to be programmed .p0, .p1 and .p2.

5.7. Integrating Gen III controllers with uDAS

From a spares point of view it is important that each camera that is converted can still be used on the original Gen II system. This means that each camera needs two sets of utility and timing lod files. This then raises the question of how uDAS knows which set to use. uDAS as it stands has no way of knowing if a Gen II or Gen III system is attached. This will need to be changed. One neat way to do this is to make use of the existing camera ID word. This ID code has its lower 8 bits set by links on the ID connector screwed to the side of each camera cryostat. These bits are read at startup by the utility boot code and the values placed in the lower 8 bits of the status word at location Y:0. Bits 8 and 9 of this status word are used to indicate shutter status. It should be possible to then use bit 10 as a flag that a GenIII controller is attached. This bit is normally set with a Gen II controller. The Gen III utility boot file would make sure it was cleared at startup.
uDAS reads the value of Util Y:0 prior to downloading the lod files, on the basis of bit 10 it could then decide which set of lod files to use.

An alternative method would be to implement a new command 'GEN' that does not appear in the GenII controller command table. A Gen III system would return '3' in response to this command, a Gen II would simply return 'ERR'.

Both of these possibilities have been implemented in the GenIII code in anticipation of the eventual uDAS modifications.

5.8. Camera source code locations

All the ING camera source code is in the dspdev account. The original Gen II code was in the following directories:
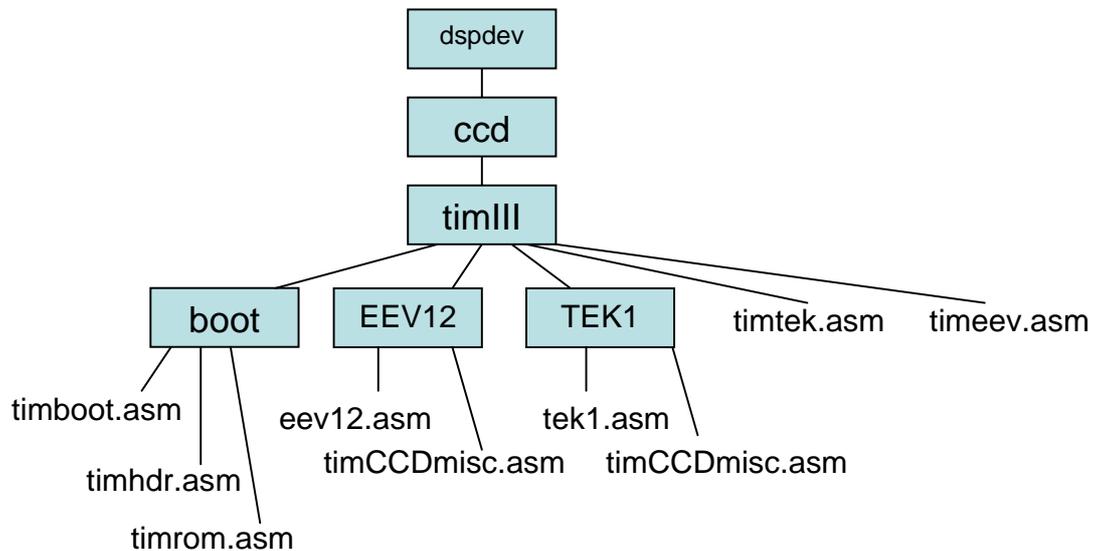
    Timing code : /home/dspdev/ccd/tim
    Utility code : /home/dspdev/ccd/util

Additional directories have been created to contain the Gen III code :

    Timing code : /home/dspdev/ccd/timIII
    Utility code : /home/dspdev/ccd/utilIII
    PCi card code : /home/dspdev/ccd/PCI_III

5.9. Source Code Structure

The structure used by ARC has been adopted. This consists of 3 .asm source files for each camera application

```
                        dspdev
                          |
                         ccd
                          |
                        timIII
          _____|_____
         |        |         |          |           |
       boot     EEV12      TEK1    timtek.asm   timeev.asm
       /|\       /\         |\
      / | \     /  \        | \
timboot.asm eev12.asm    tek1.asm
      |      timCCDmisc.asm  timCCDmisc.asm
  timhdr.asm
      |
  timrom.asm
```

In this example there are only two cameras shown. The 'EEV12' directory contains the files specific to that camera i.e. files concerned with defining its waveforms and voltages. The next level up contains a file called 'timeev.asm' which is also included in the assembly. This contains code common to all EEV cameras. The assembler also includes the files in the boot directory during assembly. 'timhdr.asm' defines all the register locations specific to the DSP56303 processor.

6.Useful web links

Astronomical Research Cameras: http://www.astro-cam.com/
Freescale semiconductor: http://www.freescale.com/