EDO12
Clock Pulse Generator

Upgrade PCB Description

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Specification Summary

Clock Input : 1 MHz from Time Service
Output Frequency Range : 0. 1 to 51. 1 Hz in 0. 1 Hz increments
Output Pulse Width : 500ns (adjustable by component change)
Maximum Jitter : +20-10 microseconds above 10 Hz
LAM : Set on each output pulse
Outputs : 4 x single ended (Lemo 00)
: 4 x line driver (Lemo 0 Tri-ax)
Frequency Setting : by CAMAC command F16A0, data binary 1 to 511

CAMAC Commands :		
F0A0	Read data register	Q = 1
F16A0	Overwrite data register	Q = 1
F8A15	Test LAM	Q = 1 if LAM set
F9A1	Clear rate multiplier and filter	
F10A15	Clear LAM	
F24A15	Disable LAM	
F26A15	Enable LAM	
F27A15	Test LAM enabled	Q = 1 if enabled
F24A1	Disable rate multiplier	
F26A1	Enable rate multiplier	
F27A1	Test rate multiplier enabled	Q = 1 if enabled
Z	Initialise	
X	1 returned for all valid commands	

(copied from J.V. Smith 27th June 1986)

Circuit Description

General

The ed012 is a single width CAMAC module that provides 8 pulsed output signals at a software selectable frequency derived from the time service 1Mhz clock input. The frequency range is 0.1 to 51.1 Hz in 0.1Hz increments and a pulse width of 0.5microseconds. The 8 signals are divided into two groups, giving 4 TTL and 4 line driver outputs. Each of the 4 TTL outputs can be inverted using an on-board selector switch. All external connections are made via the front panel, an 'N' (station selected) indicator is mounted at the top of the panel.

Frequency selection

Three quad 'D' latches, IC's 4,5&6 are used to buffer 9-bit binary data written from the CAMAC write bus . The contents of the latches can be read back onto the CAMAC read bus via IC's1,2&3. The latched binary code, converted to BCD by IC's7,8,9&10 are used to program three cascaded synchronous decade rate multiplier's (i.e. programmable counters) formed by IC's11,12,13&14 to produce rates from 0.001fin (LSB set) to 0.511fin, where fin is the input frequency of 1Mhz (note: the upper rate is actually limited by the 9-bit binary data input i.e. 2^9=512, otherwise the multiplier theoretical max is 0.999fin). Output from the rate multiplier is then applied to the first stage of four synchronous decade counters IC15,16,17&18 cascaded to 'filter' the input frequency by 10^4 counts i.e. the output frequency with the LSB set is;

$$0.001 \times 1e6Mhz/10^4 = 0.1Hz$$

This gives a frequency increment of 0.1Hz/bit. The square wave frequency output of the counter is converted to pulsed output by IC19 and fed to the output buffers via sw1-4 to IC20 and directly to IC21&22, the LAM register IC23 is 'set' on each output pulse.

CAMAC Control

Decodes

Function and Address codes generated by CAMAC are combined using TTL logic to provide;

- Q & X responses for tests and valid commands.
- Control I/O to/from the Read/Write bus.
- Enable/Disable the rate multiplier.
- Control the LAM (look-at-me) output.

Data from the Function and Address bus are buffered by IC39 & IC41 into decoder chips IC40 & 42, the 'F' & 'A' decodes are subsequently gated via IC's 24,25 and 26 to form the various control functions as above.

The data input buffer and rate multiplier are reset when a 'Z' is asserted, similarly the rate multiplier alone is cleared on assertion of an F9A1 command.

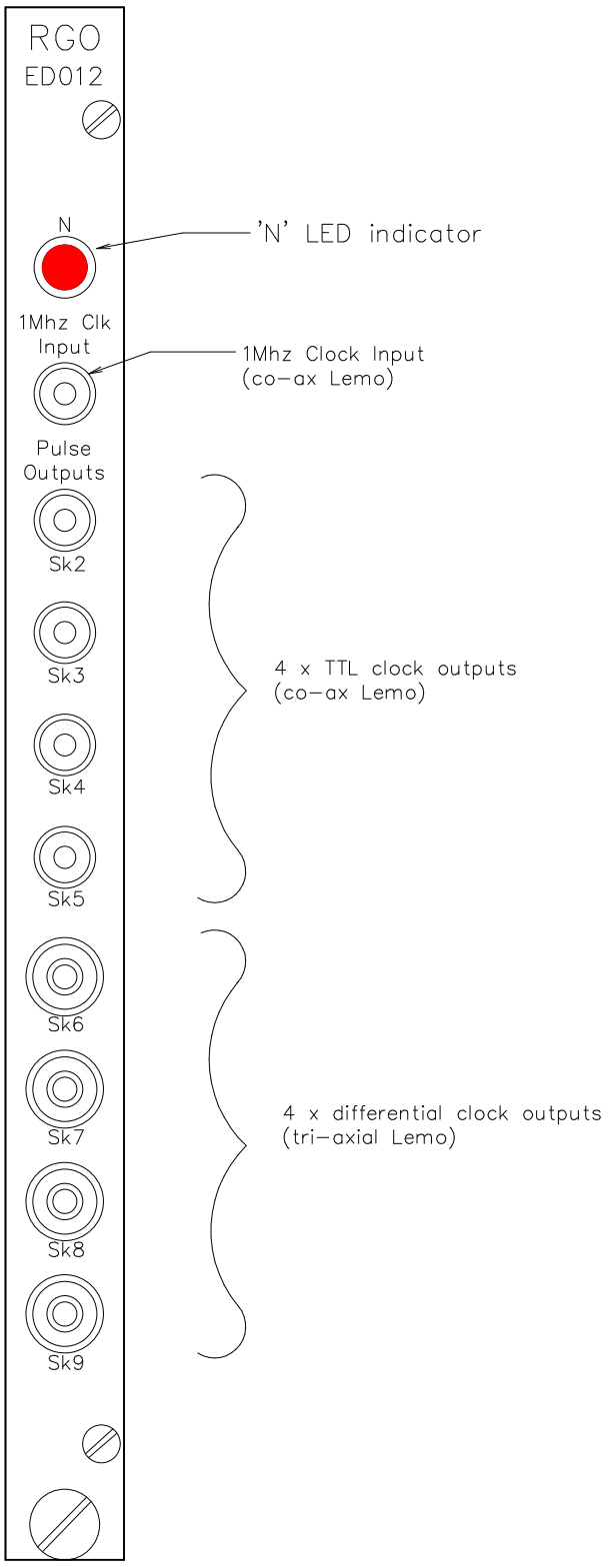
Counter/LAM control

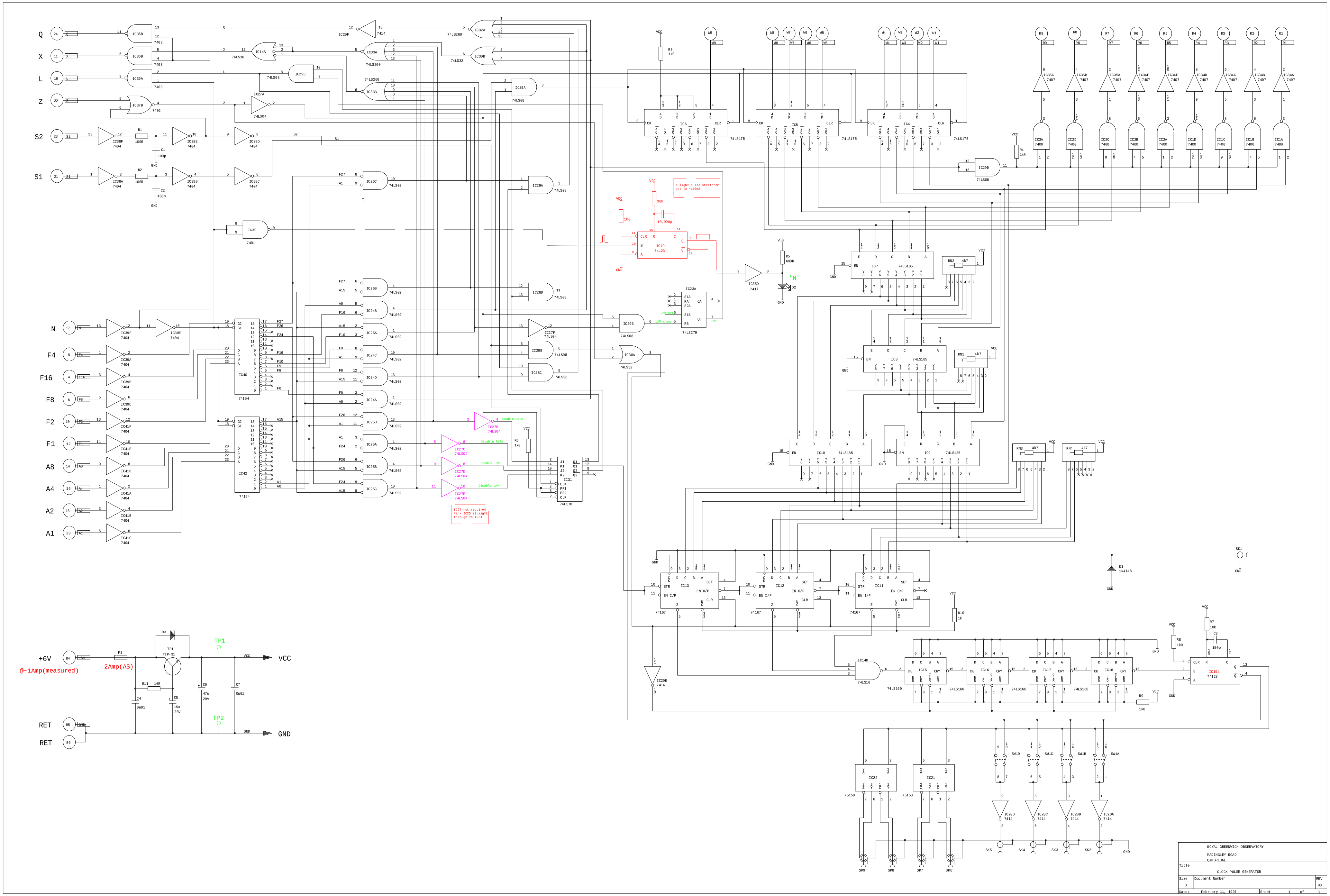
Control of the counter and LAM functions are performed by IC31 (dual J-K flip-flop). The trailing edge of CAMAC strobe S2 is used to clock the data at the J-K inputs and set the Q output accordingly. The quiescent 'low', asserted on the J-K input when no function is selected, prevent any further change on subsequent clock pulses.

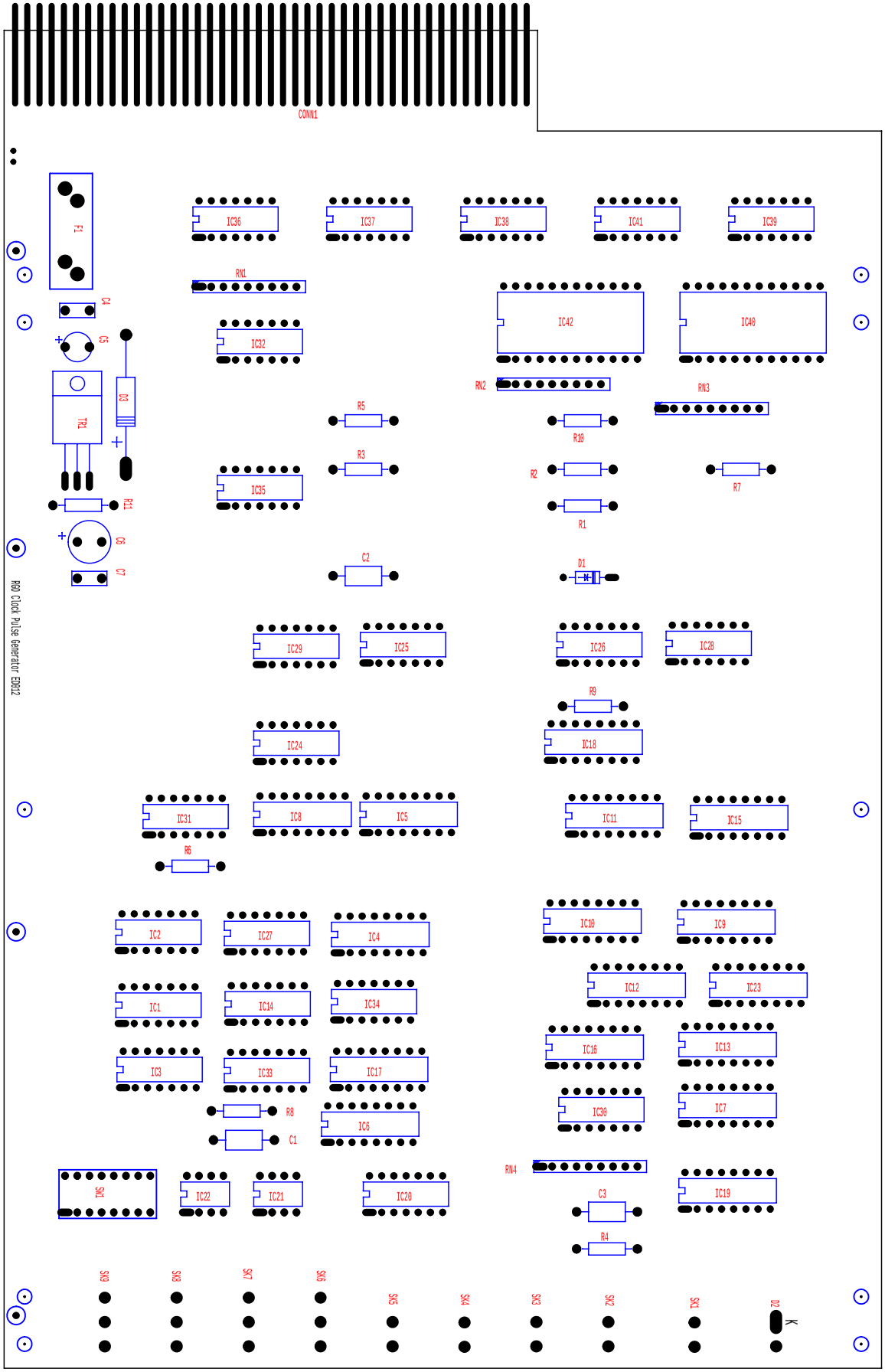
LAM function

The LAM function for this module is used to set the TCS sample rate. The output signal of the rate multiplier (counter) derived from IC19p4 is used to set S-R latch IC23p6. The output of IC23p7 is further gated via IC29c (LAM enable) and IC36a ('N') to form a valid LAM signal to the CAMAC system. The normal response to the LAM is to generate an F10A15 code which, after gating, asserts a LAM clear signal at IC23p5 and thus the process is allowed to repeat itself.

Camac Clock Pulse Generator.
(ED012 module)




Q
X
L
Z
S2
S1
N
F4
F16
F8
F2
F1
A8
A4
A2
A1
+6V
@~1Amp(measured)
2Amp(AS)
RET
RET
VCC
GND
TP1
TP2
ROYAL GREENWICH OBSERVATORY
MADINGLEY ROAD
CAMBRIDGE
Title
CLOCK PULSE GENERATOR
Size D
Document Number
REV 03
Date: February 11, 1997
Sheet 1 of 1


CONN1
F1
C4
C5
TR1
D3
R11
C6
C7
IC36
IC37
IC38
IC41
IC39
RN1
IC32
IC42
IC40
RN2
RN3
R5
R10
R3
IC35
R2
R7
R1
C2
D1
IC29
IC25
IC26
IC28
R9
IC24
IC18
IC31
IC8
IC5
IC11
IC15
R6
IC2
IC27
IC4
IC10
IC9
IC1
IC14
IC34
IC12
IC23
IC3
IC33
IC17
IC16
IC13
IC30
IC7
R8
C1
IC6
SW1
IC22
IC21
IC20
RN4
C3
IC19
R4
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
D2
R80 Clock Pulse Generator ED012