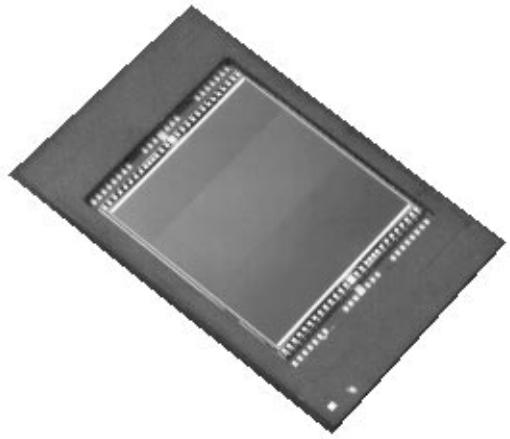
Marconi Applied Technologies
CCD05-30 Inverted Mode Sensor
High Performance CCD Sensor

FEATURES

- 1242 (H) by 1152 (V) Pixel Format
- 28 by 26 mm Active Area
- Extremely Low Pixel Readout Noise
- Visible Light and X-Ray Sensitive
- Uniform Response over Whole Image Area
- Low Noise Amplifier for Slow-Scan Systems and Large Signal Amplifier for High Speed Applications
- Symmetrical Anti-Static Gate Protection
- Radiation Tolerant
- Advanced Inverted Mode Operation



INTRODUCTION

The CCD05-30 is one of the CCD05 range of very large area CCD image sensors primarily intended to suit the requirements of astronomy, medical diagnostic and scientific measuring instruments. Standard three-phase clocking and buried channel charge transfer are employed. The device operates in the inverted mode for minimum dark current. The readout register has a high performance low noise amplifier at one end for slow-scan applications and a high speed amplifier at the other end. The image area is split into two sections which can be clocked separately for frame transfer operation.

The CCD05-30 series scientific image sensor is primarily specified for operation in a full-frame imaging mode with slow-scan readout from the whole image area through the low noise amplifier and is tested at a temperature of approximately 253 K.

Other operating modes are also possible, including use of the high speed amplifier (but at higher noise) and pixel binning. Potential users are invited to discuss their applications with Marconi Applied Technologies to ensure optimum performance.

In common with all other Marconi Applied Technologies CCD sensors, the CCD05-30 is available with a fibre-optic window or taper, a UV coating or a phosphor coating for hard X-ray detection.

Designers are advised to consult Marconi Applied Technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE
(Low noise amplifier)

Pixel readout frequency	20 – 1500	kHz
Output amplifier sensitivity	2.0	$\mu V/e^-$
Peak signal	300	ke^-/pixel
Dynamic range	50 000:1	
Spectral range	420 – 1060	nm
Readout noise (at 140 K, 20 kHz)	6	e^- rms
Q.E. at 700 nm	45	%
Peak output voltage	0.6	V

GENERAL DATA

Format

Image region (section A)	1242(H) x 576(V)	pixels
Image region (section B)	1242(H) x 576(V)	pixels
Image area (sections A + B)	27.95 x 25.92	mm
Pixel pitch (row and column)	22.5 x 22.5	µm

Package

Outline dimensions	53.3 x 33.0 mm
Number of pins	44
Inter-pin spacing	2.54 mm
Inter-row spacing	2.54 mm
Inner row spacing (across sensor)	43.18 mm
Window	removable glass
Mounting position	any

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PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	150k	300k	-	e^-/pixel
Peak output voltage (unbinned)	-	0.6	-	V
Dark signal at 293 K (see note 2)	-	200	400	e^-/pixel/s
Charge transfer efficiency (see note 3):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier sensitivity:				
low noise amplifier	-	2.0	-	$\mu V/e^-$
high speed amplifier	-	0.6	-	$\mu V/e^-$
Readout noise at 253 K (see note 4) (low noise amplifier):				
grade 0	-	6	8	rms e^-/pixel
grade 1	-	8	10	rms e^-/pixel
Readout frequency (see note 5):				
low noise amplifier	-	50	1500	kHz
high speed amplifier	-	1000	15000	kHz
Response non-uniformity (std. deviation)	-	3	10	% of mean
Dark signal non-uniformity at 293 K (std. deviation, σ)	-	80	160	e^-/pixel/s
Output node capacity relative to image section:				
towards low noise amplifier	-	2.0	-	
towards high speed amplifier	-	4.0	-	

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level):

	Min	Typical	Max	
I∅/I∅ interphase	-	18	-	nF
R∅/R∅ interphase	-	110	-	pF
I∅/SS	-	50	-	nF
R∅/SS	-	240	-	pF
Output impedance (low noise amplifier):				
∅R on	-	1.8	-	kΩ
∅R off	-	2.8	-	kΩ
Output impedance (high speed amplifier):				
∅R on	-	0.8	-	kΩ
∅R off	-	1.5	-	kΩ

NOTES

1. Signal level at which resolution begins to degrade.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 and 300 K is given by:

   $$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
4. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period. Due to the high output impedance of the CCD05-30, these noise levels will only be achieved with a very low input current amplifier.
5. Readout above the values specified may be achieved but performance to the parameters given cannot be guaranteed.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 253 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots $>10\%$ contrast at half saturation, 253 K.

White spots Are counted when they have a generation rate 100 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 273 K). The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by:

$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 9 white defects.

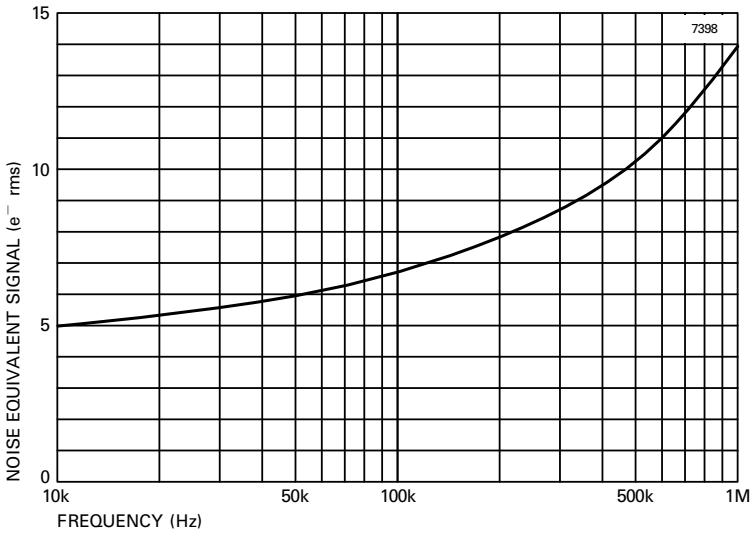
Black column A column which contains at least 9 black defects.

GRADE	0	1	2
Column defects:			
black or slipped	0	2	6
white	0	0	0
Traps >200 e^-	2	5	12
White spots	42	42	65
Black spots	20	40	200

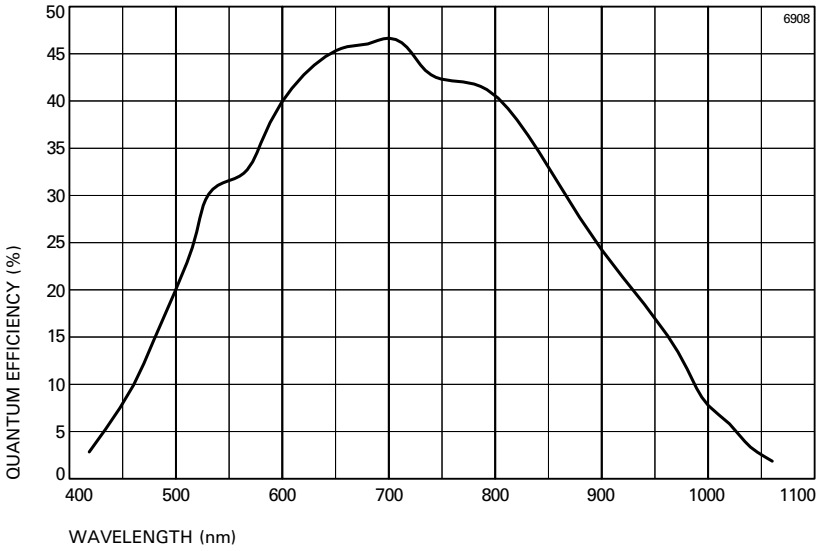
Minimum separation between adjacent black columns . . . . . 50 pixels

Note The effect of temperature on defects is that traps will be less noticeable at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

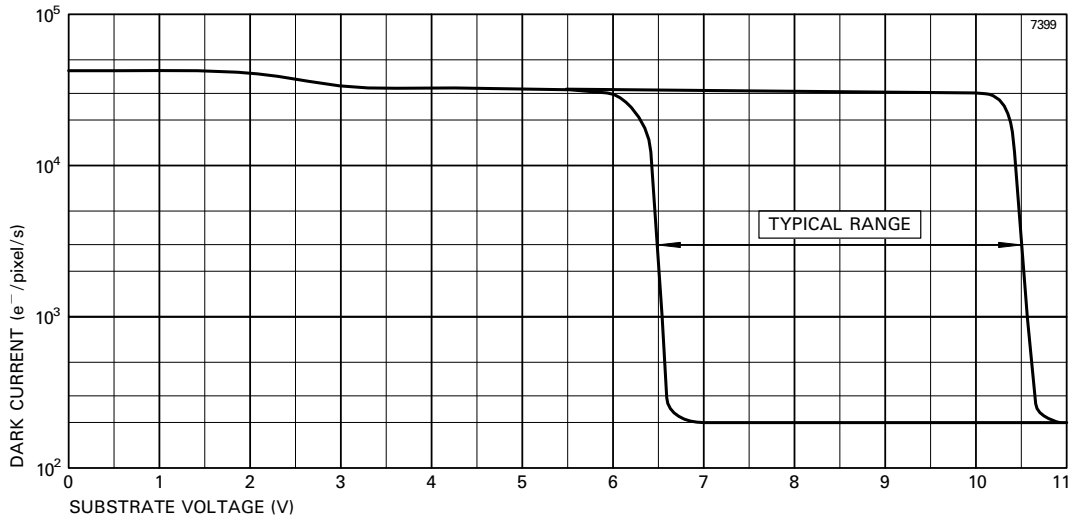
TYPICAL OUTPUT CIRCUIT NOISE (Measured using clamp and sample)



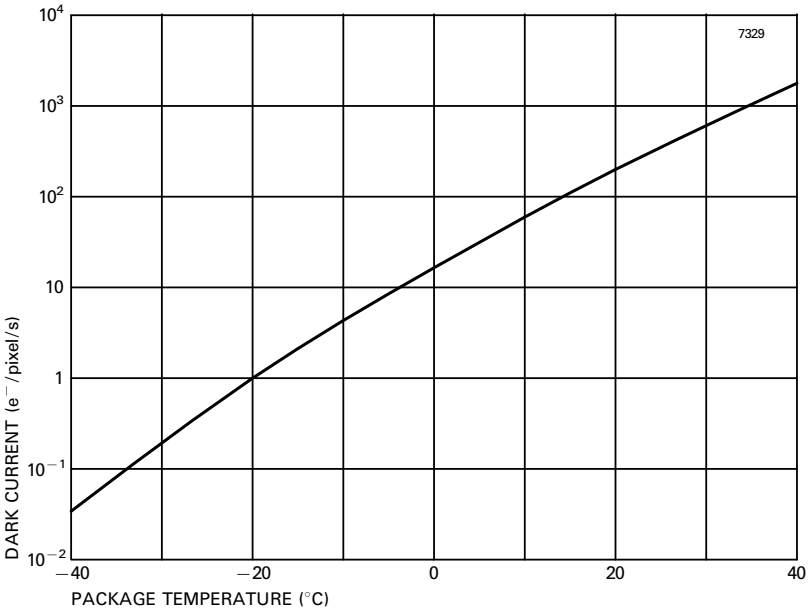
TYPICAL SPECTRAL RESPONSE (No window)



TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE



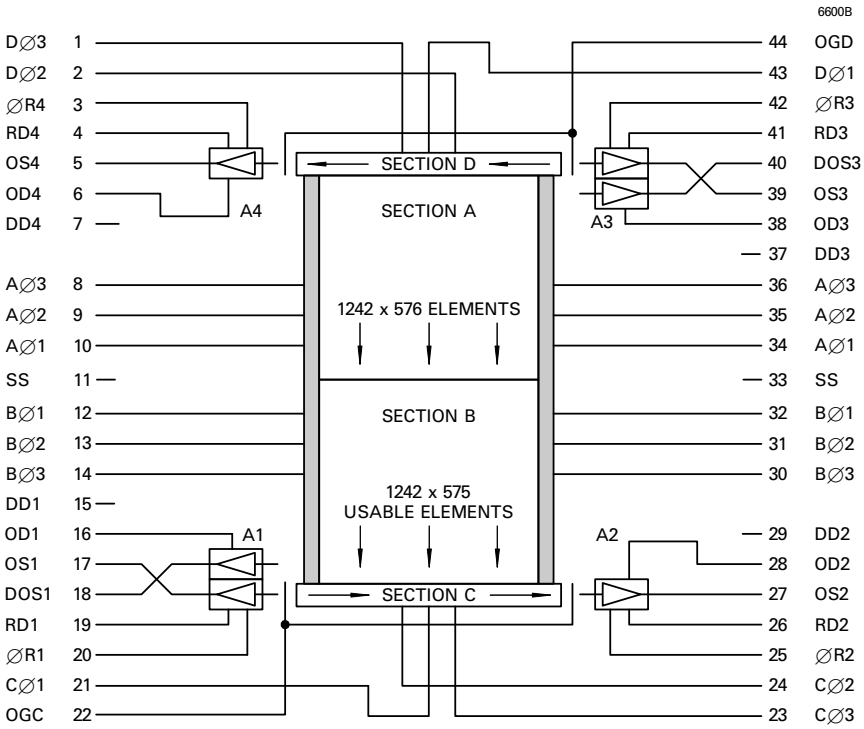
TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC

Arrows show direction of charge transfer with clock phases connected as shown. In AIMO devices, charge can only be transferred through sections A and B towards C. This means that section D and amplifiers A3 and A4 are redundant.

The charge detection amplifier A1 is optimised for large signal, high speed operation, whereas amplifier A2 is optimised for very low noise under cooled slow-scan operation.



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6) Min	Typical	Max	MAXIMUM RATINGS with respect to V_{SS}
1	D∅3	D register readout (see note 7)	0	0	0	±20 V
2	D∅2	D register readout (see note 7)	0	0	0	±20 V
3	∅R4	Output reset pulse (see note 7)	0	0	0	±20 V
4	RD4	Reset transistor drain (see note 7)	20	22	25	−0.3 to +25 V
5	OS4	Output transistor source (see note 7)	20	22	25	−0.3 to +25 V
6	OD4	Output transistor drain (see note 7)	20	22	25	−0.3 to +25 V
7	DD4	Diode drain (see note 7)	20	22	25	−0.3 to +25 V
8	A∅3	Section A drive pulse	10	12	15	±20 V
9	A∅2	Section A drive pulse	10	12	15	±20 V
10	A∅1	Section A drive pulse	10	12	15	±20 V
11	SS	Substrate (see note 8)	8	9.5	10.5	-
12	B∅1	Section B drive pulse	10	12	15	±20 V
13	B∅2	Section B drive pulse	10	12	15	±20 V
14	B∅3	Section B drive pulse	10	12	15	±20 V
15	DD1	Diode drain	20	22	25	−0.3 to +25 V
16	OD1	Output drains (A1)	20	22	25	−0.3 to +25 V
17	OS1	Output transistor source (A1)	see note 9			−0.3 to +25 V
18	DOS1	Dummy output source (A1)	see note 9			−0.3 to +25 V
19	RD1	Reset transistor drain (A1)	15	17	19	−0.3 to +25 V
20	∅R1	Output reset pulse (A1)	8	12	15	±20 V
21	C∅1	C register readout (see note 10)	10	12	15	±20 V
22	OGC	C register output gate	2	3	5	±20 V
23	C∅3	C register readout (see note 10)	10	12	15	±20 V
24	C∅2	C register readout (see note 10)	10	12	15	±20 V
25	∅R2	Output reset pulse (A2)	8	12	15	±20 V
26	RD2	Reset transistor drain (A2)	15	17	22	−0.3 to +25 V
27	OS2	Output transistor source (A2)	see note 11			−0.3 to +25 V
28	OD2	Output transistor drain (A2)	27	29	30	−0.3 to +25 V
29	DD2	Diode drain	20	22	25	−0.3 to +25 V
30	B∅3	Section B drive pulse	10	12	15	±20 V
31	B∅2	Section B drive pulse	10	12	15	±20 V
32	B∅1	Section B drive pulse	10	12	15	±20 V
33	SS	Substrate (see note 8)	8	9.5	10.5	-
34	A∅1	Section A drive pulse	10	12	15	±20 V
35	A∅2	Section A drive pulse	10	12	15	±20 V
36	A∅3	Section A drive pulse	10	12	15	±20 V
37	DD3	Diode drain	20	22	25	−0.3 to +25 V
38	OD3	Output drains (A3) (see note 7)	20	22	25	−0.3 to +25 V
39	OS3	Output transistor source (A3) (see note 7)	20	22	25	−0.3 to +25 V
40	DOS3	Dummy output source (A3) (see note 7)	20	22	25	−0.3 to +25 V
41	RD3	Reset transistor drain (A3) (see note 7)	20	22	25	−0.3 to +25 V
42	∅R3	Output reset pulse (A3) (see note 7)	0	0	0	±20 V
43	D∅1	D register readout (see note 7)	0	0	0	±20 V
44	OGD	D register output gate (see note 7)	0	0	0	±20 V

Voltages between pairs of pins:

pin 5 (OS4) to pin 6 (OD4)	±15	V
pin 16 (OD1) to pin 17 (OS1)	±15	V
pin 16 (OD1) to pin 18 (DOS1)	±15	V
pin 27 (OS2) to pin 28 (OD2)	±15	V
pin 38 (OD3) to pin 39 (OS3)	±15	V
pin 38 (OD3) to pin 40 (DOS3)	±15	V
Current through any source or drain pin	10	mA

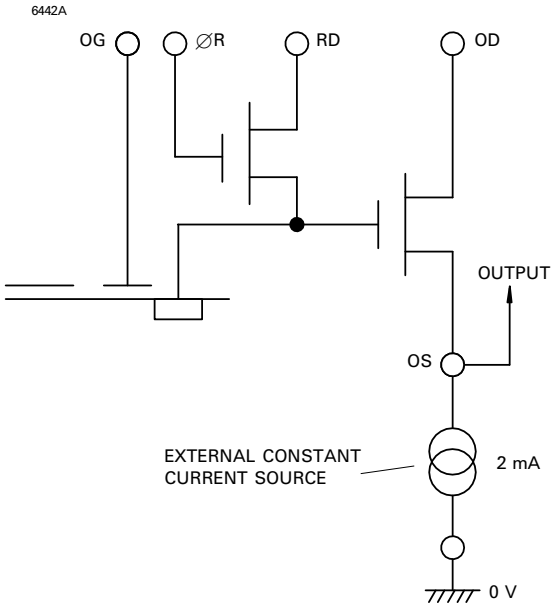
Operation at the typical voltages should give performance at, or close to, the specification limits. Some adjustment within the specified range may be required to optimise performance.

NOTES

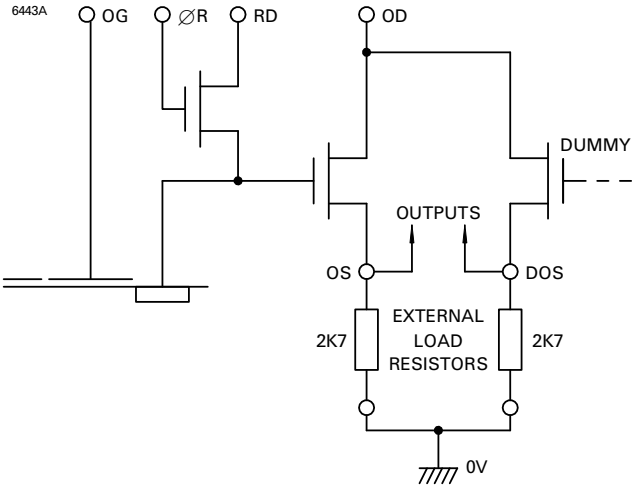
6. All image clock low levels 0 ± 0.5 V. Other clock low levels + 1 V.
7. The AIMO variant of the CCD05-30 can only transfer charge towards the section C register. Therefore the section D register and A3/A4 output circuits are not used.
8. The substrate voltage may need to be adjusted within the range indicated to achieve correct inverted mode operation.
9. With 2.7 kΩ load resistors, $V_{OS} = V_{DOS} = V_{RD} - 3$ V.
10. Readout through amplifier 2 shown; for readout through amplifier 1, C∅1 and C∅2 should be interchanged.
11. With a 2 mA constant current load, $V_{OS} = V_{RD} + 6$ V.

OUTPUT AMPLIFIER SCHEMATICS

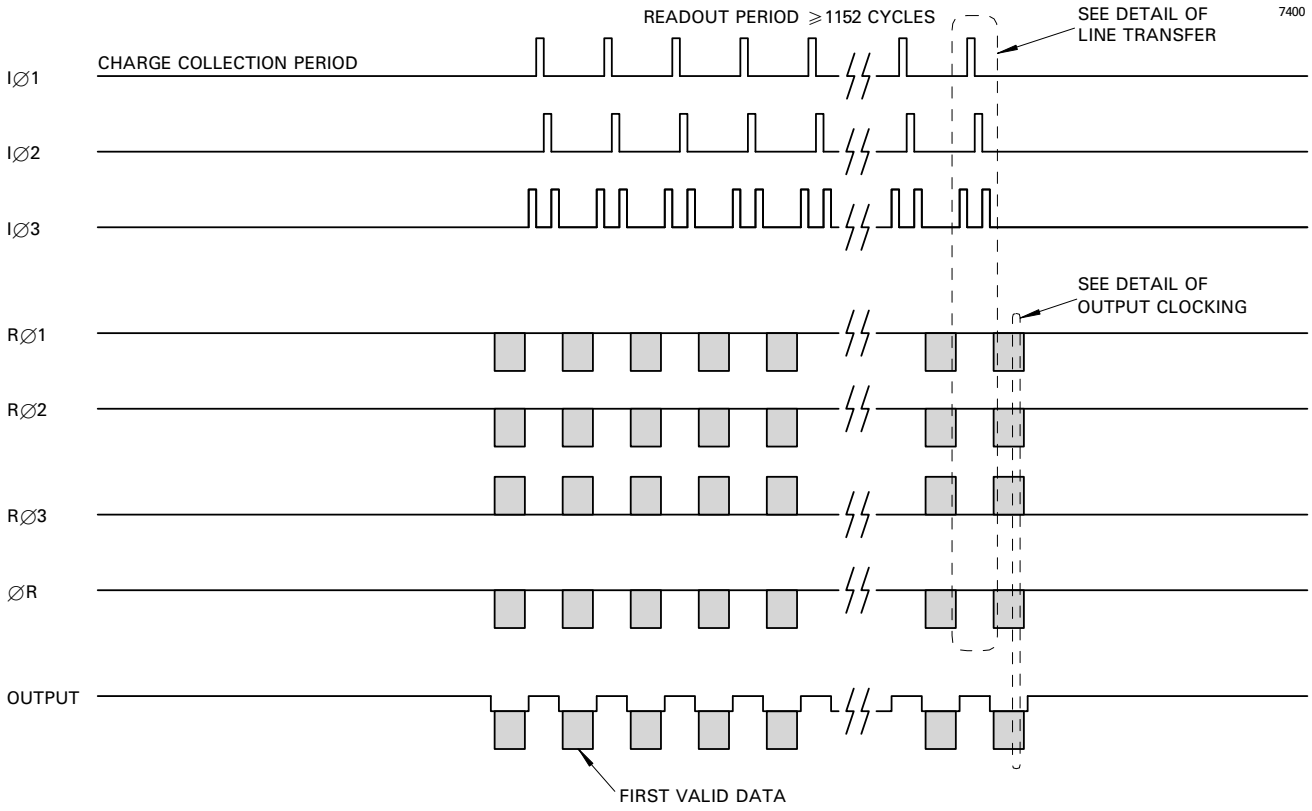
Low Noise (A2)



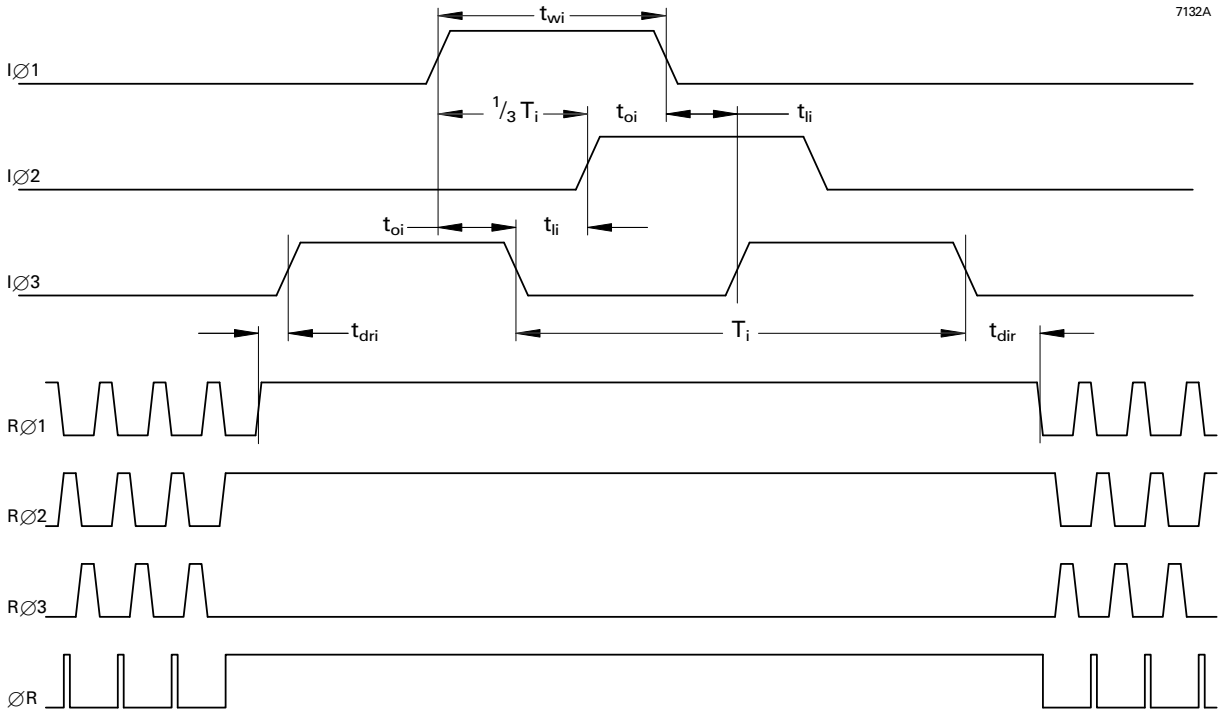
High Speed (A1)



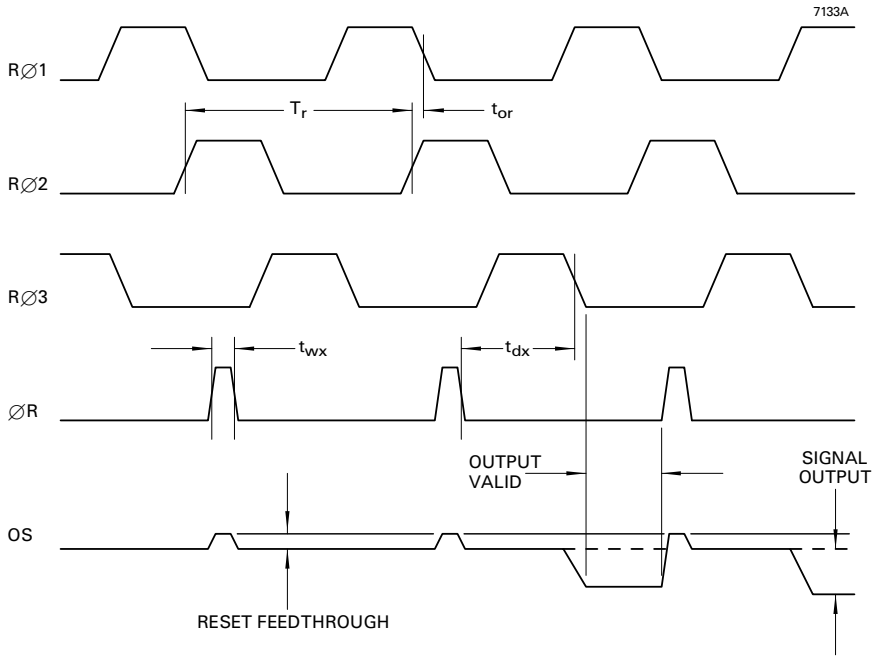
FRAME READOUT TIMING DIAGRAM



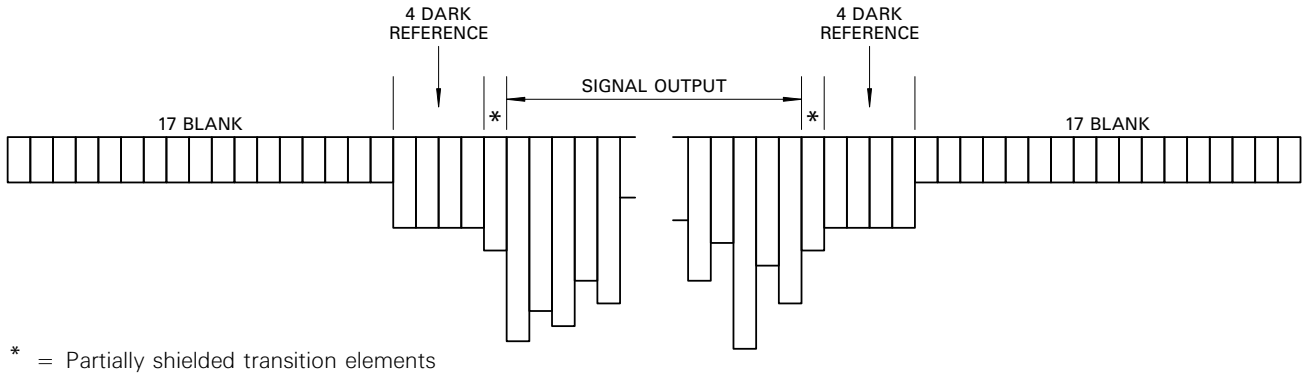
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



* = Partially shielded transition elements

CLOCK TIMING REQUIREMENTS

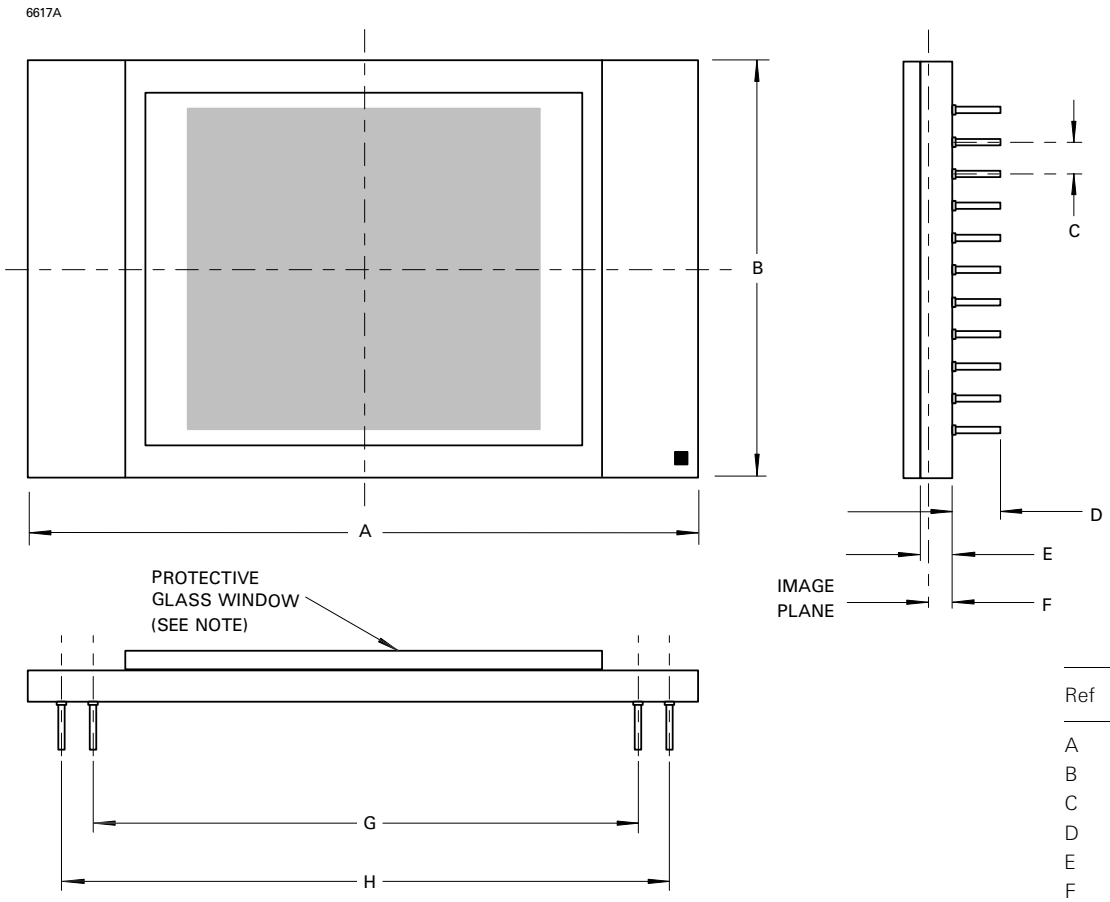
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	15	30	see note 12	µs
t_{wi}	Image clock pulse width	7	15	see note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	2	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	2	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	5	see note 12	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 12	µs
T_r	Output register clock cycle period	200	see note 13	see note 12	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
13. As set by the readout period.

OUTLINE (All dimensions nominal)

Not for inspection purposes

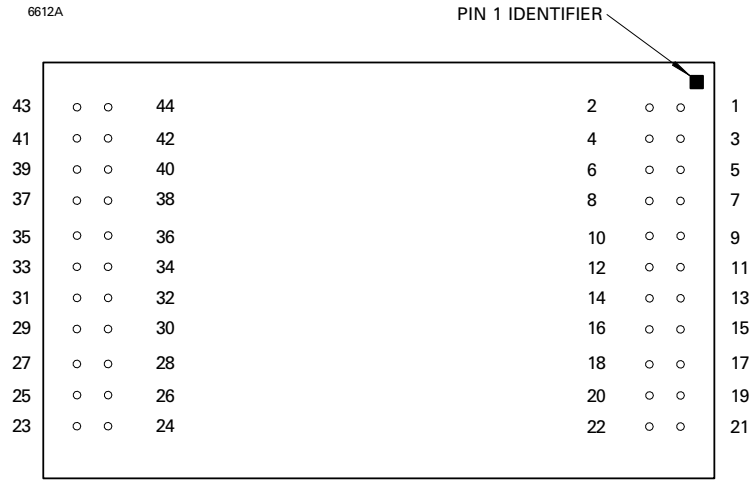


Ref	Millimetres
A	53.34
B	33.02
C	2.54
D	3.81
E	2.29
F	1.68
G	43.18
H	48.26

Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

PIN CONNECTIONS (View on Pins)



ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact Marconi Applied Technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 1, 2, 3, 8, 9, 10, 12, 13, 14, 20, 21, 22, 23, 24, 25, 30, 31, 32, 34, 35, 36, 42, 43, 44) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at Marconi Applied Technologies. Users planning to use CCDs in a high radiation environment are advised to contact Marconi Applied Technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min