REDplus4 28th February 2014

CCD	Function	Cryo A 20-41	Cryo B 20-41	Front A 27W2	Front B 27W2	Vid A	Vid B	ClkA	ClkB	Bias	Clock	Notes
SubD con1		For final voltage values see SDSU code										
1	SS	Y		13		Pin22				0V		substrate
2	DOS-E	f										disconnected (no load res.) if DOD-E powered down
3	OS-E	W		A1		SMA J2				10KΩ		video output E
4	OG-E	A		11		Pin 9				2.5v		Set to 2.5v for mode 1
5	DG-A	F		16				Pin13(P) CLK12			12v/0v	Sits at 0v, requires 12v pulse for charge dump during clear
6	ΦR-E	U		8				Pin1(S) CLK0			12v/0v	reset clock E
7	SWΦ-E	T		20				Pin2(S) CLK1			10v/0v	Summing well E
8	E1	h		7				Pin3(S) CLK2			10v/0v	RΦ1
9	E2	S		19				Pin4(S) CLK3			10v/0v	RΦ2
10	E3-F3	R		6				Pin5(S) CLK4			10v/0v	RΦ3
11	F1	P		18				Pin6(S) CLK5			10v/0v	RΦ1
12	F2	N		5				Pin7(S) CLK6			10v/0v	RΦ2
13	SWΦ-F	q		17				Pin8(S) CLK7			10v/0v	Summing well F
14	ΦR-F	M		4				Pin9(S) CLK8			12v/0v	reset clock F
15	TG-A	L		3				Pin14(P) CLK13			10v/0v	Clocked as IΦ4 or kept low depending on direction of charge transfer
16	OG-F	C		12		Pin 10				2.5v		Set to 2.5v for mode 1
17	OS-F	a		A2		SMA J4				10KΩ		video output F
18	DOS-F	g										disconnected (no load resistor) if DOD-F is powered down
19	SS	k		13		Pin22				0v		substrate
20	DOD-E	m		13		Pin22				0v		Dummy OS powered down
21	RD-E	D		24		Pin 5				17v		Reset Drain E
22	OD-E	j		10		Pin 1				27.5		Output Drain E
23	SS	n		13		Pin22				0v		substrate
24	A4	J		15				Pin15(P) CLK14			10v/0v	$I\Phi_4$
25	A3	d		2				Pin16(P) CLK15			10v/0v	$I\Phi_3$
26	B4	K		15				Pin15(P) CLK14			10v/0v	$I\Phi_4$
27	B3	e		2				Pin16(P) CLK15			10v/0v	$I\Phi_3$
28	SS	p		13		Pin22				0v		substrate
29	DD-A	V		23		Pin 2				29v		Dump drain A
30	B1	H		14				Pin17(P) CLK16			10v/0v	$I\Phi_1$
31	B2	c		1				Pin18(P) CLK17			10v/0v	$I\Phi_2$
32	A1	G		14				Pin17(P) CLK16			10v/0v	$I\Phi_1$
33	A2	b		1				Pin18(P) CLK17			10v/0v	$I\Phi_2$
34	SS	s		13		Pin22				0v		substrate
35	OD-F	X		10		Pin 1				27.5v		Output Drain F
36	RD-F	B		25		Pin 8				17v		Reset Drain F
37	DOD-F	t		13		Pin22				0v		Dummy OS powered down
				21								Chassis ground

SubD con 2

1	SS		Y		13		Pin 22			0v		substrate
2	DOS-G		f									disconnected (no load resistor) if DOD-G is powered down
3	OS-G		W		A1		SMA J2			10KΩ		video output G
4	OG-G		A		11		Pin 9			2.5v		Set to 2.5v for mode 1
5	DG-D		F		16				Pin13(P) CLK12		12v/0v	Sits at 0v, requires 12v pulse for charge dump during clear
6	ΦR-G		U		8				Pin1(S) CLK0		12v/0v	reset clock G
7	SWΦ-G		T		20				Pin2(S) CLK1		10v/0v	Summing well G
8	G1		h		7				Pin3(S) CLK2		10v/0v	RΦ1
9	G2		S		19				Pin4(S) CLK3		10v/0v	RΦ2
10	G3-H3		R		6				Pin5(S) CLK4		10v/0v	RΦ3
11	H1		P		18				Pin6(S) CLK5		10v/0v	RΦ1
12	H2		N		5				Pin7(S) CLK6		10v/0v	RΦ2
13	SWΦ-H		q		17				Pin8(S) CLK7		10v/0v	Summing well H
14	ΦR-H		M		4				Pin9(S) CLK8		12v/0v	reset clock H
15	TG-D		L		3				Pin14(P) CLK13		12v/0v	Clocked as IΦ1 or kept low depending on direction of charge transfer
16	OG-H		C		12		Pin 10			2.5v		Set to 2.5v for mode 1
17	OS-H		a		A2		SMA J4			10KΩ		video output H
18	DOS-H		g									disconnected (no load resistor) if DOD-H is powered down
19	SS		k		13		Pin22			0v		substrate
20	DOD-G		m		13		Pin22			0v		Dummy OS powered down
21	RD-G		D		24		Pin 5			17v		Reset Drain G
22	OD-G		j		10		Pin 1			27.5v		Output Drain G
23	SS		n		13		Pin22			0v		substrate
24	D1		J		15				Pin17(P) CLK16		10v/0v	$I\Phi_1$
25	D2		d		2				Pin18 (P) CLK17		10v/0v	$I\Phi_2$
26	C1		K		15				Pin17(P) CLK16		10v/0v	$I\Phi_1$
27	C2		e		2				Pin18 (P) CLK17		10v/0v	$I\Phi_2$
28	SS		p		13		Pin22			0v		substrate
29	DD-D		V		23		Pin 2			29v		Dump drain D
30	C4		H		14				Pin15 (P) CLK14		10v/0v	$I\Phi_4$
31	C3		c		1				Pin16 (P) CLK15		10v/0v	$I\Phi_3$
32	D4		G		14				Pin15 (P) CLK14		10v/0v	$I\Phi_4$
33	D3		b		1				Pin16 (P) CLK15		10v/0v	$I\Phi_3$
34	SS		s		13		Pin22			0v		substrate
35	OD-H		X		10		Pin1			27.5v		Output Drain H
36	RD-H		B		25		Pin 8			17v		Reset Drain H
37	DOD-H		t		13		Pin22			0v		Dummy OS powered down
					21							Chassis ground

Notes:

1) Use 'mode 1' for lowest read noise (mode 2 has higher storage capacity)
2) Vss is split between video cards by CCD connector ? (should they go to 1 card)
3) Device will be read out in split full frame readout through diagonally opposite corners to minimise cross-talk, or through a single output & binned
4) Not used in differential mode so dummy outputs are powered down.
5) ODs on same register paralleled up as not in use at same time, if in use at the same time they would need to be separate to be able to independantly optimise each Output
6) Independant DDs (should they be commoned up)
7) Independent DGs in case only one register is used.
8) Check serial clocks to ensure clocking direction can be reversed to use alternative pair of amps
9) TGs clocked independently just in case a bad register needs to be isolated.
10) Parallel clock phases different between connectors think about for code
11) Will not be moved in FT mode so common up C/D and A/B
12) SWs clocked independently just in case a bad amp needs to be isolated
13) Is there any benefit from commoning up serial clocks or diag. opposite reset clocks ?